

FLORIDA INTERNATIONAL UNIVERSITY

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

EEL 6167: VLSI DESIGN

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AIM-SPICE TUTORIAL

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TABLE OF CONTENTS

1. INTRODUCTION.....	3
2. ABOUT THE TOOL.....	3
2.1 THE USER INTERFACE.....	4
3. DESIGN AND NETLIST.....	5
3.1 GETTING STARTED	5
3.2 INPUT DATA FOR CIRCUIT DESCRIPTION.....	5
3.3 REPRESENTATION AND SYNTAX OF BASIC COMPONENTS.....	6
3.4 CREATING NETLIST.....	7
4. SIMULATION.....	8
4.1 AC SIMULATION SYNTAX.....	9
4.2 DC SIMULATION SYNTAX.....	9
4.3 TRANSIENT SIMULATION SYNTAX.....	9
4.4 DISPLAY	10
5. EDITING.....	12
REFERENCES.....	13

LIST OF FIGURES

Figure 1 – AIM-Spice command window.....	3
Figure 2 – Toolbar.....	4
Figure 3 – Inverter circuit schematic.....	7
Figure 4 – Aim-Spice net list.....	8
Figure 5 – AC simulation window.....	8
Figure 6 – DC simulation window.....	9
Figure 7 – Transient simulation window.....	10
Figure 8 – Output of inverter circuit.....	10
Figure 9 – Plot window.....	11
Figure 10 – 2-Input NAND circuit schematic.....	12
Figure 11 – Error window.....	12

1. INTRODUCTION

The tutorial explains basic concepts associated with utilizing the Automatic Integrated Circuit Modeling Spice (AIM-Spice) for circuit simulations. This simulation tool is a version of SPICE that can run on Microsoft Windows operating systems, including Windows NT, Windows 2000 and Windows X. This tutorial will provide explanations helpful in using the simulator for defining circuit designs, generating circuit netlists, running the simulation and displaying the output of the simulation. Appropriate examples are also included to help users understand simulation techniques.

2. ABOUT THE TOOL

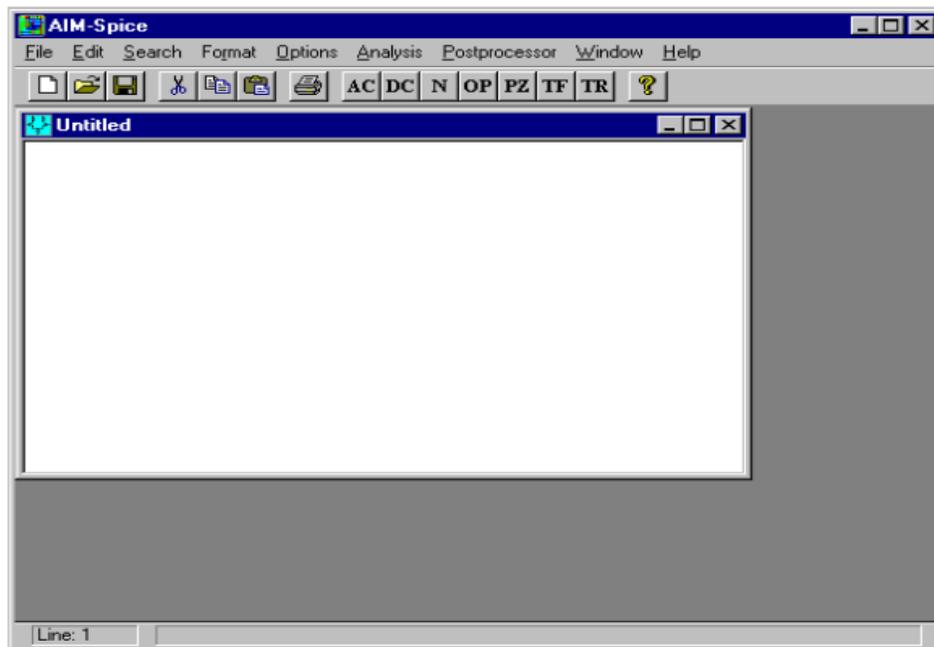


Figure 1 – AIM-Spice command window

2.1 THE USER INTERFACE

A. The Command Window

This is the part of the tool that is used to display the command window, commands, system variables, options, and messages. The prompt is noticeable in this resizable window.

B. Menus and Toolbars

Menus and toolbars for access to simulation analysis & commands, settings, and modes are shown below.

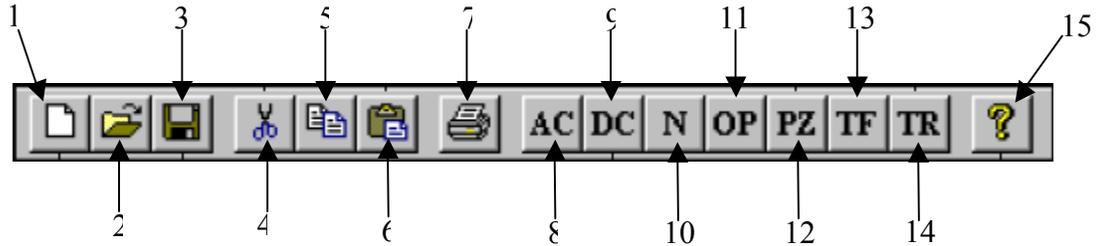


Figure 2 – Toolbar

- | | | |
|--------------|---------------------|---------------------------------|
| 1 – New page | 6 – Paste | 11 – Operating Point Analysis |
| 2 – Open | 7 – Print | 12 – Pole Zero Analysis |
| 3 – Save | 8 – AC Analysis | 13 – Transfer Function Analysis |
| 4 – Cut | 9 – DC Analysis | 14 – Transient Analysis |
| 5 – Copy | 10 – Noise Analysis | 15 – Help |

C. Pointing Devices

The main pointing device for the tool is a mouse, click on the drop-down menu or toolbar buttons on the simulator window to use the respective functions.

3. DESIGN AND NETLIST

3.1 GETTING STARTED

1. Start the Aim-Spice program by clicking on new page button on the command window.
2. To open an existing netlist click the open button and select the desired file.

3.2 INPUT DATA FOR CIRCUIT DESCRIPTION

In order to simulate a circuit, a schematic diagram of the circuit is needed to determine the nodes that define every device that is part of the circuit. A Device/Element must be uniquely labeled, and the nodes must be numbered with nonnegative integers for example a node may be labeled as “1 0” with “0” indicating ground, and “1” indicating a terminal that is positive with respect to ground. After the nodes and the devices that are defined by each set of nodes have been identified, the circuit is then described in a sequence of lines. The sequence of lines consist of statements that are responsible for definition of signal or power supply sources, single element or device, model parameters, specification of output to be analyzed or analysis types. Input format is as follows:

Circuit Title
Power Supplies
Signal Sources
Device/Element Descriptions
Model Statements

The first line is the “Circuit Title” to identify the type of function or type of circuit being simulated. The power supplies and signal sources indicate what type of input the circuit requires, this may be AC, DC, or transient input type. The “Device/Element” line is where the devices that make up the design are listed with respect to the nodes defining each one of the devices. The “Model Statement” indicates what model of device is being used in the simulation.

In order to run the simulation with devices that have specific models, the model commands have to be included with a “dot” in front of the model command line.

3.3 REPRESENTATION AND SYNTAX OF BASIC COMPONENTS

1. Resistors (R)

<RESISTOR NAME> <N+> <N-> <VALUE>

2. Capacitors (C) and Inductors (L)

<CAPACITOR NAME> <N+> <N-> <VALUE>

<INDUCTOR NAME-L> <N+> <N-> <VALUE>

3. Diode

<DIODE NAME> <N+> <N-> <DIODE MODEL NAME>

Diode Model command:

.MODEL <MODEL NAME> <DIODE TYPE> (PARAMETER)

4. Bipolar transistors

<BJT NAME - Q> <NC> <NB> <NE> <BJT MODEL NAME>

(NC – collector node, NB – base node, NE - emitter node)

BJT Model command:

.MODEL <BJT MODEL NAME> <BJT TYPE> (PARAMETER)

5. MOSFETS

<FET NAME> <ND> <NG> <NS> <NB> <MODEL NAME> <L=VALUE> <W=VALUE>

(ND - drain node, NG - gate node, NS - source node, NB - substrate node, L - length, W - width)

FET Model command:

.MODEL <MODEL NAME> <MOS TYPE> (PARAMETER)

3.4 CREATING NETLIST

Example 1 - CMOS Inverter

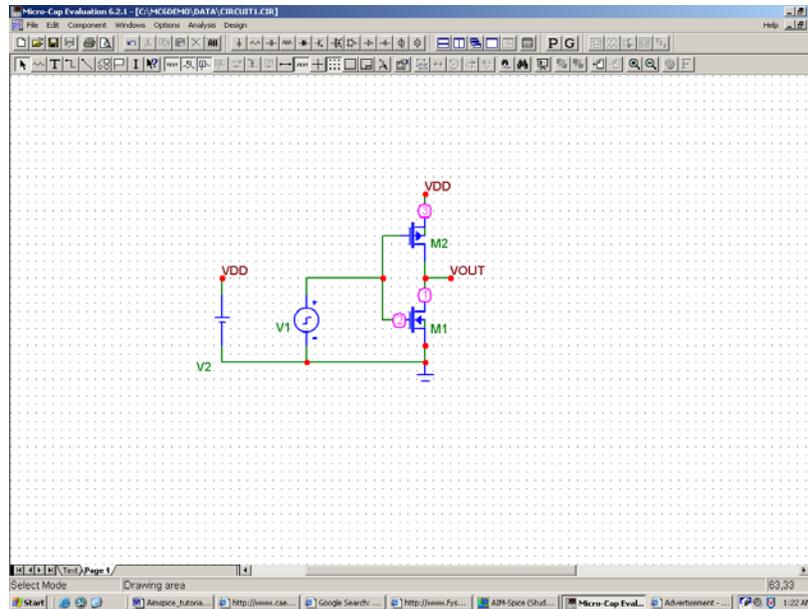


Figure 3 – Inverter circuit schematic

Figure 3 shows a PSpice circuit schematic of an inverter circuit used to indicate unique nodes for design analysis. The power supply “VDD” is defined by nodes “3 0” because it is connected to the PMOS transistor “M2”. The signal input “V1” supplies a transient (pulse) waveform and it is connected between the common input of the transistors (node 2) and ground. Figure 4 shows the command window with information to simulate the inverter. The first line has the circuit title, and the format for remaining lines is listed below.

```
<POWER SUPPLY> <N+> <N-> <VALUE>  
<SIGNAL SOURCE> <N+> <N-> <SIGNAL TYPE (SIGNAL PARAMETERS)>  
<DEVICENAME> <ND> <NG> <NS> <NB> MODELNAME <L=VALUE> <W=VALUE>  
.MODEL <MODELNAME> <MODELTYPE> <MODEL PARAMETERS>
```

The nodes are denoted by <N+> and <N->. The device terminals, in this case MOSFET with drain, gate, source and substrate/body are denoted by <ND>, <NG>, <NS> and <NB> respectively. In Figure 4, notice that the tool is not case

sensitive, as long as the syntax is correct the simulation will progress. The last line of the format starts with a bolded **“.MODEL”** to indicate that it is a command.

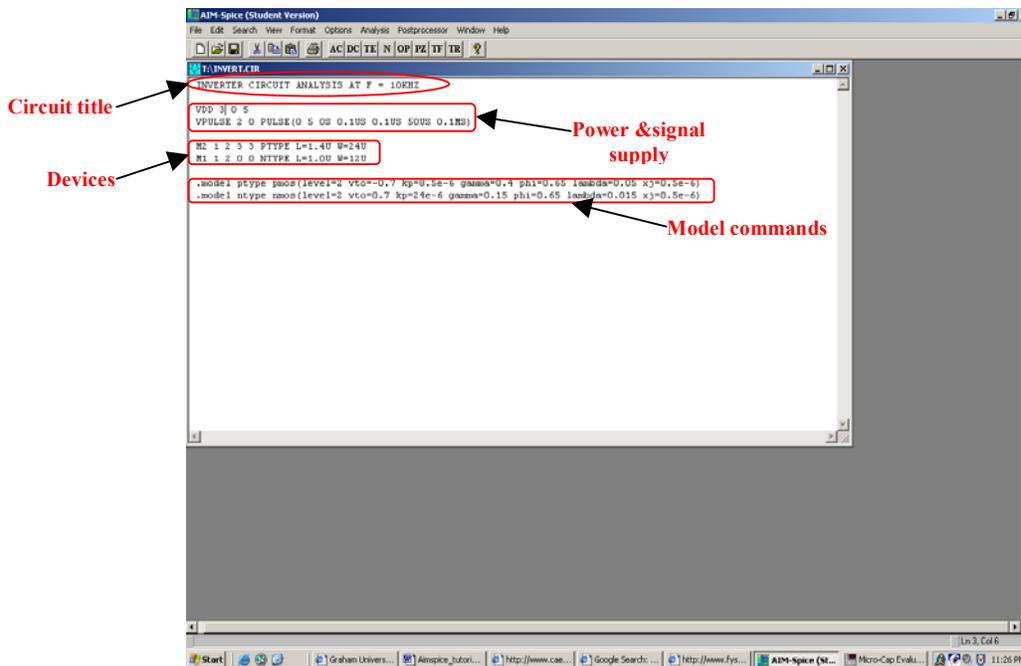


Figure 4 – Aim-Spice net list

4. SIMULATION

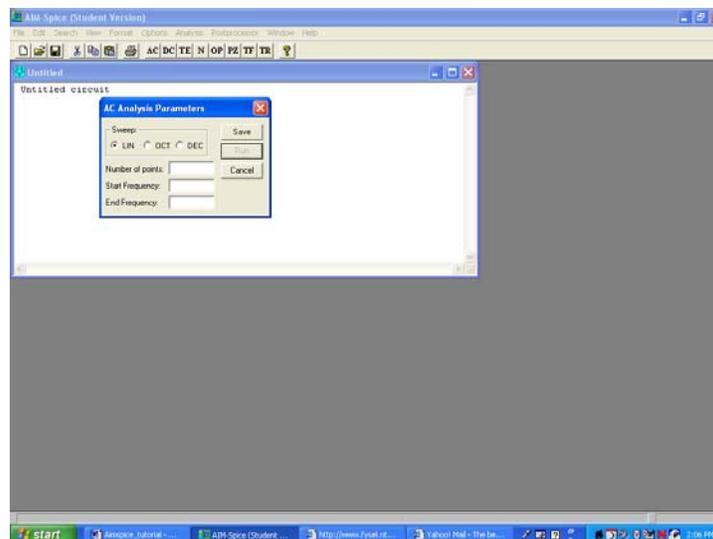


Figure 5 – AC simulation window

4.1 AC SIMULATION SYNTAX

<SOURCE NAME> <N+> <N-> SIN (V-OFFSET VAMP FREQ TD THETA PHASE) AC 1

The AC analysis window in Figure 5 is also used to specify the simulation parameters.

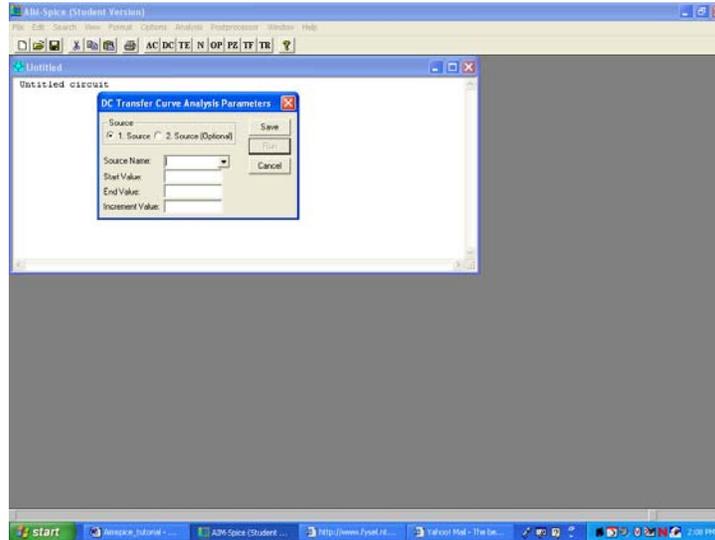


Figure 6 – DC simulation window

4.2 DC SIMULATION SYNTAX

<SOURCE NAME> <N+> <N-> <DC VALUE>

Example: VDD 1 0 10

(DC value between nodes "1" and ground is 10V)

4.3 TRANSIENT SIMULATION SYNTAX

PULSE SIGNAL

<SOURCE NAME> <N+> <N-> PULSE (V1 V2 TD TR TF PW PERIOD)

(TD - time delay, TR - rise time, TF – fall time, PW – Pulse width)

SINUSOIDAL SIGNAL

<SOURCE NAME> <N+> <N-> SIN (V-offset Vamp FREQ TD THETA)

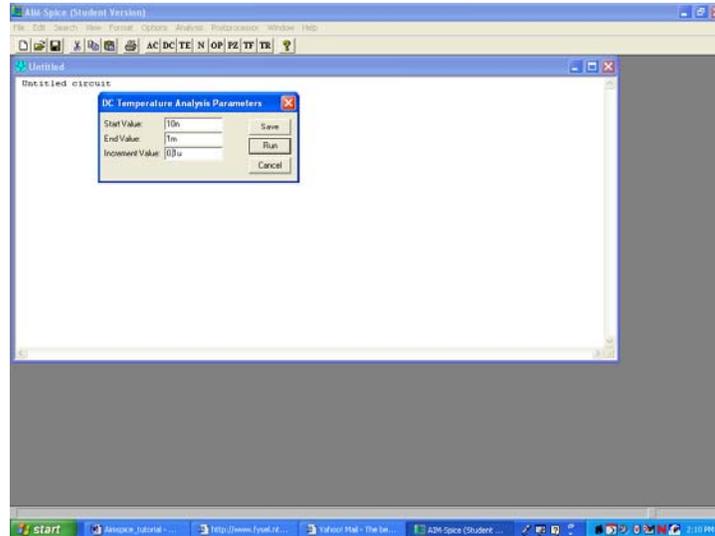


Figure 7 – Transient simulation window

4.4 DISPLAY

SAMPLE PLOT

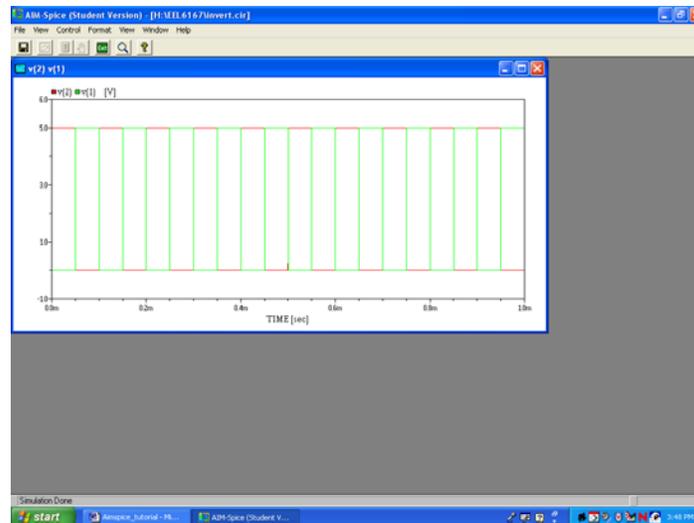


Figure 8 – Output of inverter circuit

In order to display a plot of the netlisted circuit, click on the appropriate simulation type, a window should appear. In the window, specify the parameters and values you need to simulate the circuit. Save the parameter and click “run”. After you run the program, a window will appear and you have the option of selecting a single plot or multiple plots by clicking on the desired plot and then click the “OK” button. The plot window comes up after the variable to plot has been selected.

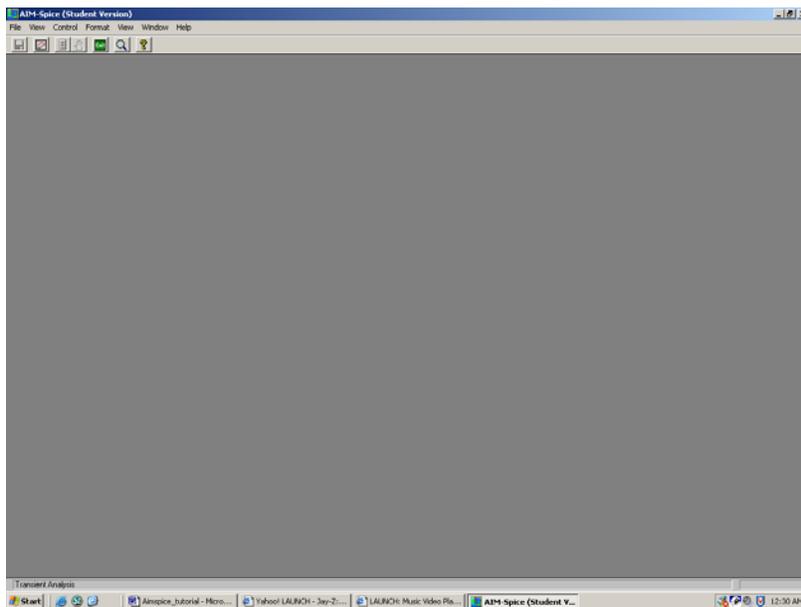


Figure 9 – Plot window

Figure 6 shows the plot window, the toolbar button with the “traffic-light” icon is used to continue the simulation. Click on the icon, you will either get another window or an error message. The window “simulation statistics” is the final pop-up window that appears, click “OK” to get the desired variable plot. The drop-down menu can be used to modify the plot. Click on the “Format” menu and modify the X or Y axis or add title and labels to the plot.

5. EDITING

Example 2 - A 2-INPUT NAND CIRCUIT

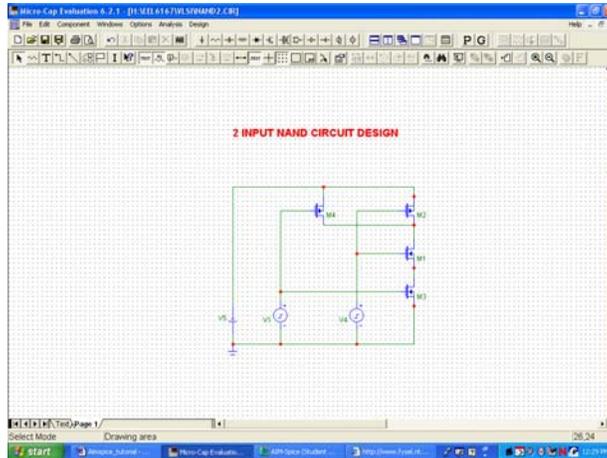


Figure 10 – 2-Input NAND circuit schematic

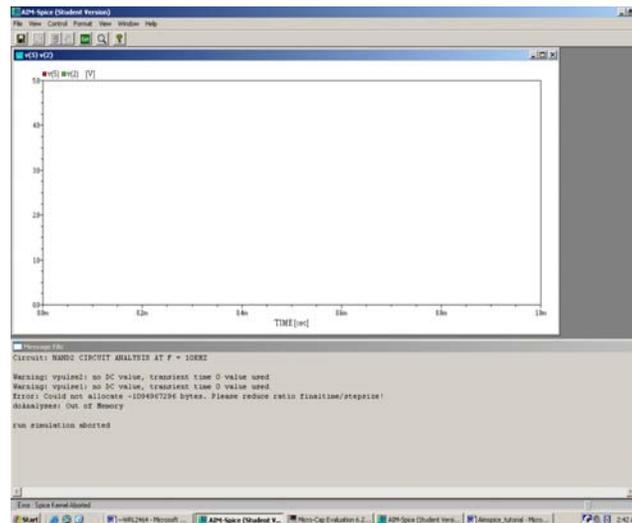


Figure 11 – Error window

Figure 6 shows a gray window that pops up as a result of error in the simulation, the lines that generate the errors are usually listed for any correction or editing of the netlist. Common mistakes are due to typos or incorrect syntax in the description of the circuit.

REFERENCES

1. <http://www.aimspice.com/>
2. <http://www.fysel.ntnu.no/Courses/tfe4185/Spiceintro/aimuser.pdf>
3. http://www.cae.wise.edu/~kime/555/tutorials/hspice/spc_tut.pdf