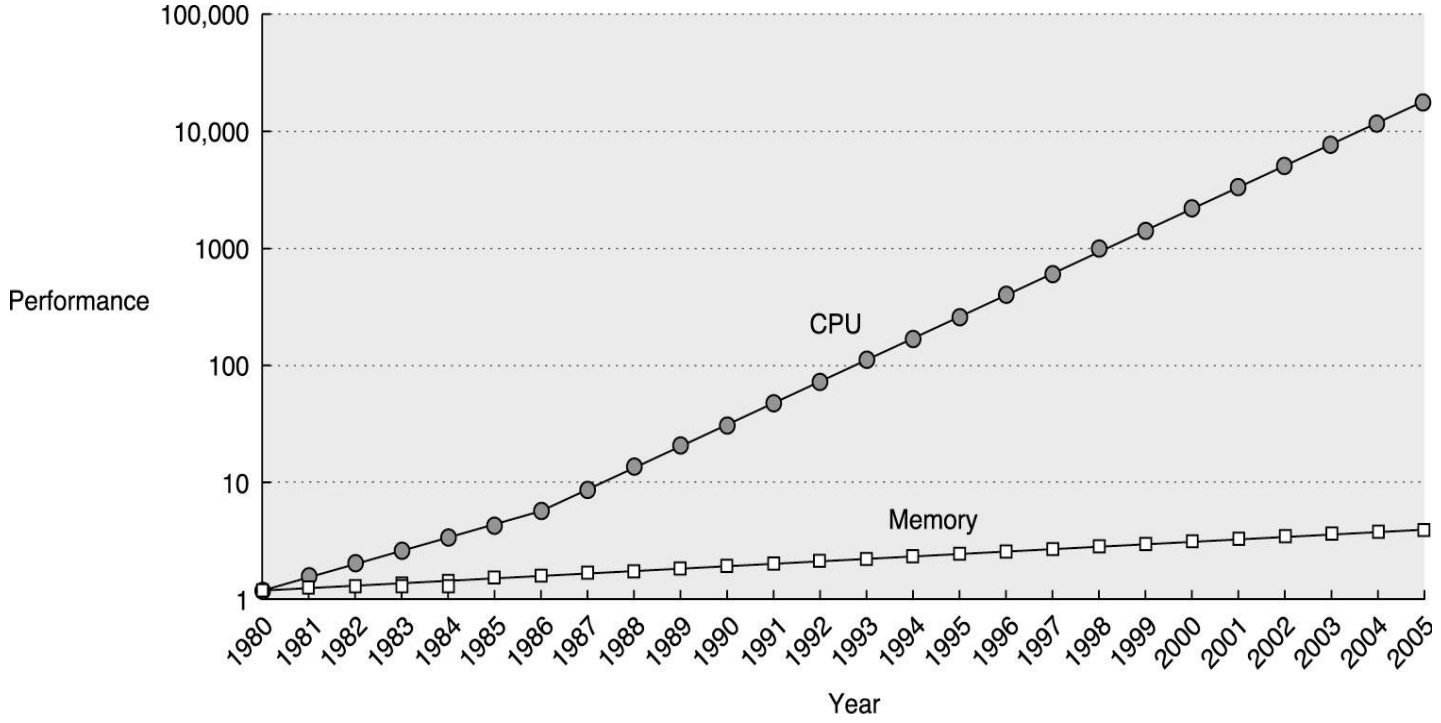
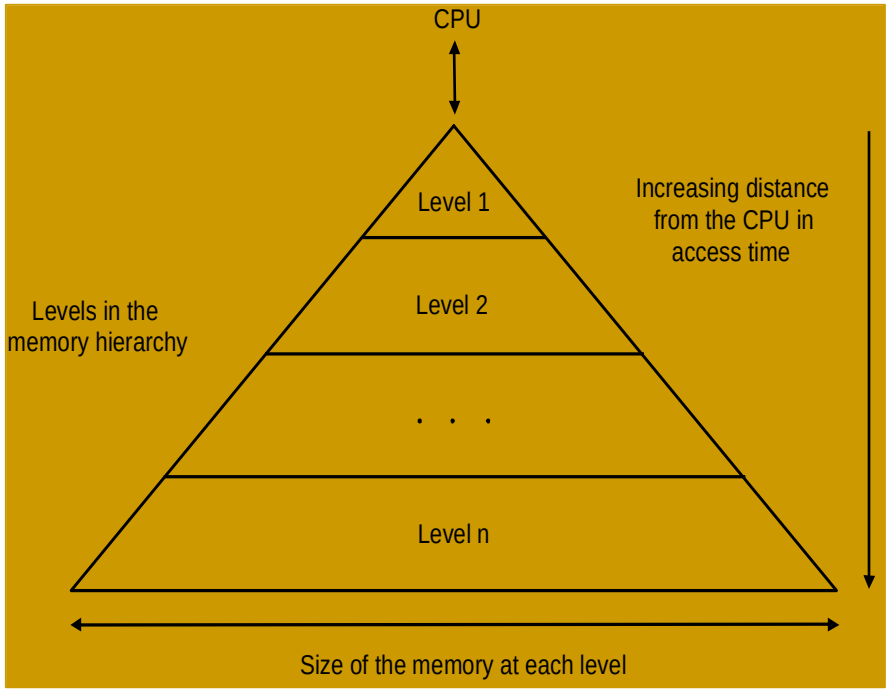
Memory

The Memory/Processor Performance Gap

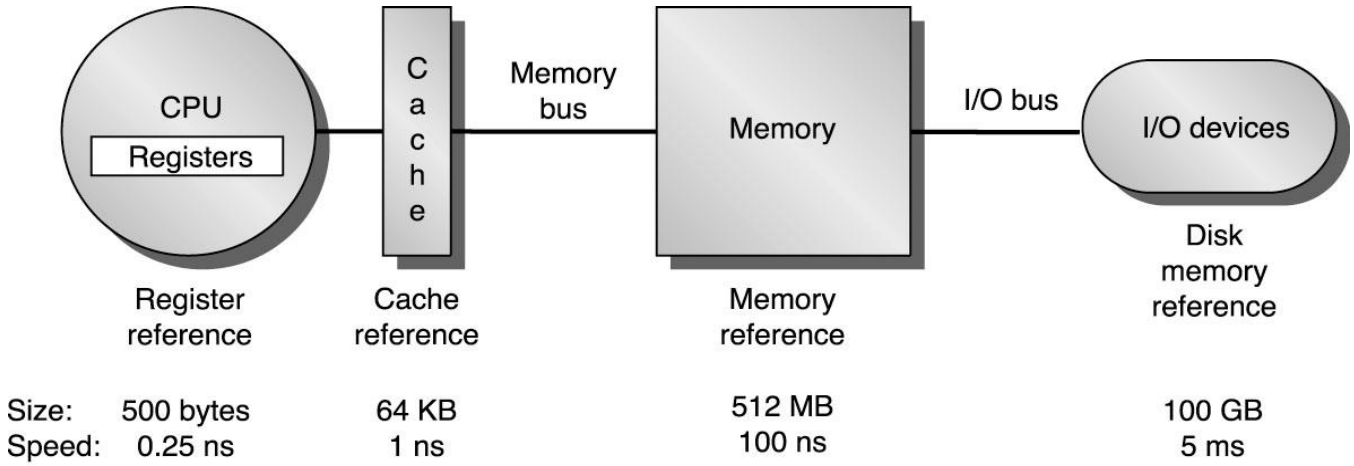


Memory-Processor Performance Gap

The memory hierarchy



The memory hierarchy

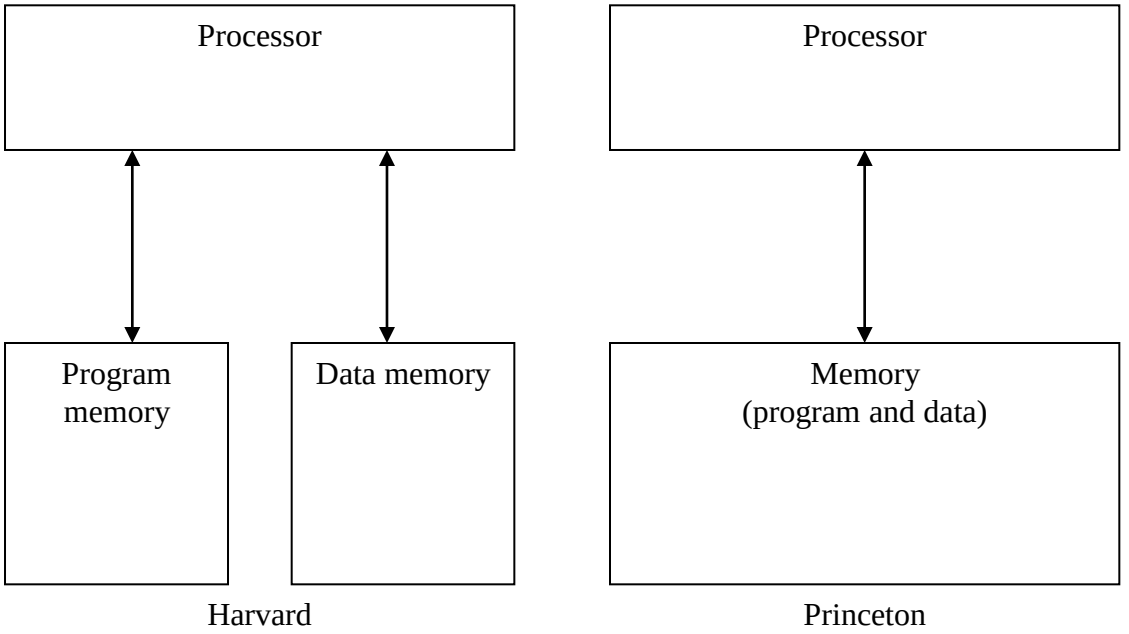


Fundamentals of Memory Hierarchy

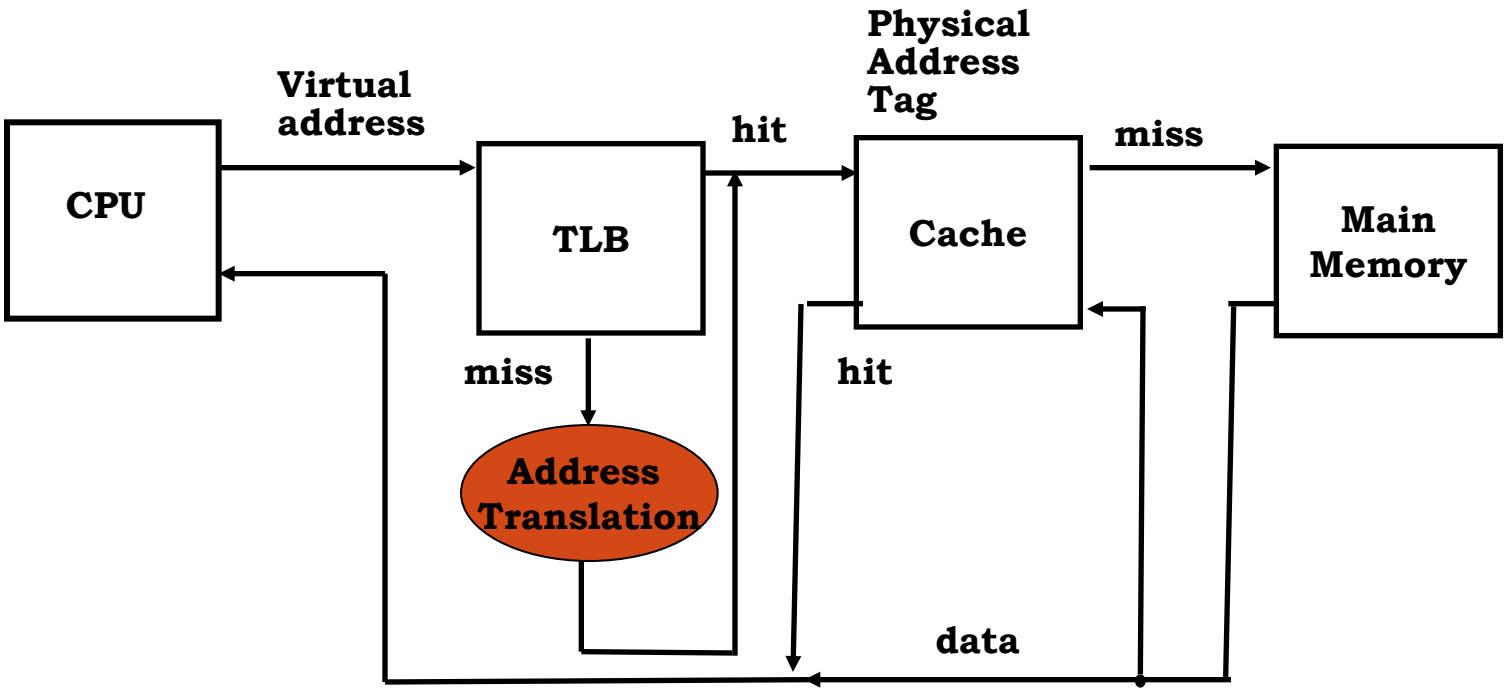
- Locality
  - Temporal locality
    - The currently required data are likely to need again in the near future
  - Spatial locality
    - There is high probability that the other data nearby will be need soon

Two Processor/Memory Architectures

- Princeton
  - Fewer memory wires
- Harvard
  - Simultaneous program and data memory access



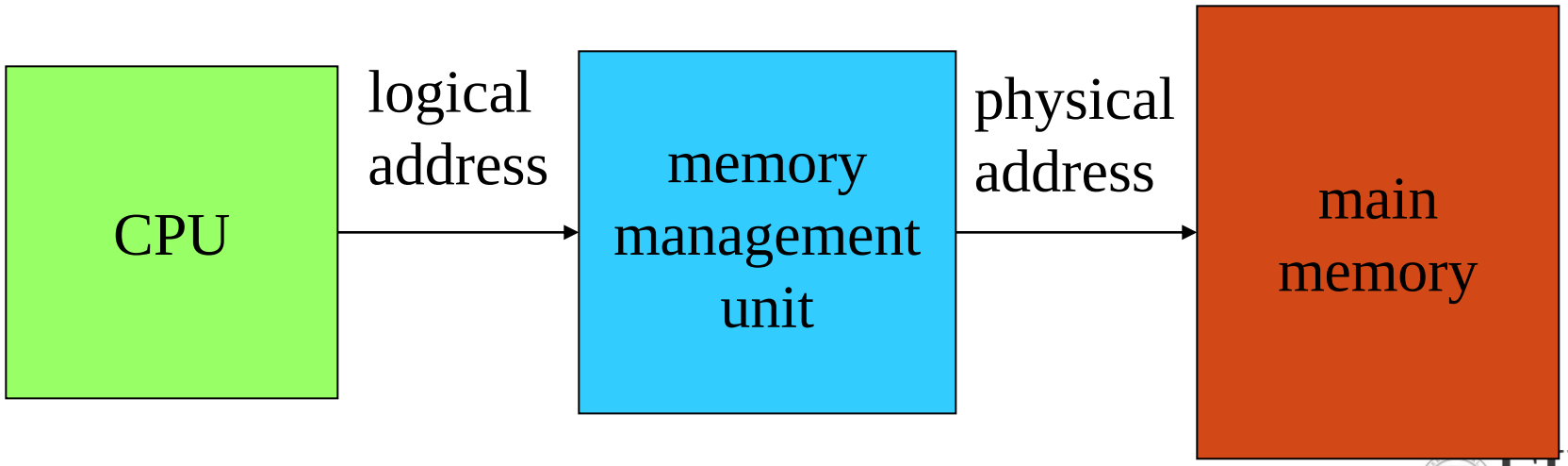
Memory Access Process



TLB (Translation lookaside buffer): Translate a virtual address to a physical address

Memory management units

- Handles DRAM refresh, bus interface and arbitration
- Takes care of memory sharing among multiple processors
- Translates logic memory addresses from processor to physical memory addresses



Memory Data Organization

- Endianness
  - Big Endian/Little Endian
- Memory data alignment

Endianness

- The order of bytes (sometimes "bit") in memory to represent different data types
- Little/Big Endian
  - Little Endian:
    - put the least-significant byte first (at lower address)
    - e.g. Intel Processor
  - Big Endian:
    - put the most-significant byte first
    - e.g.some PowerPCs, Motorola, MIPS, SPARC

Big/Little Endian Example

- 32bit data 0xFABC0123 at address 0xFF20

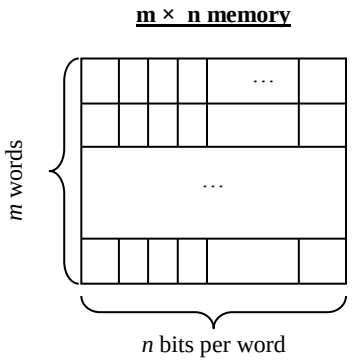
	0xFF20	0xFF21	0xFF22	0xFF23
Big Endian	0xFA	0xBC	0x01	0x23
Little Endian	0x23	0x01	0xBC	0xFA

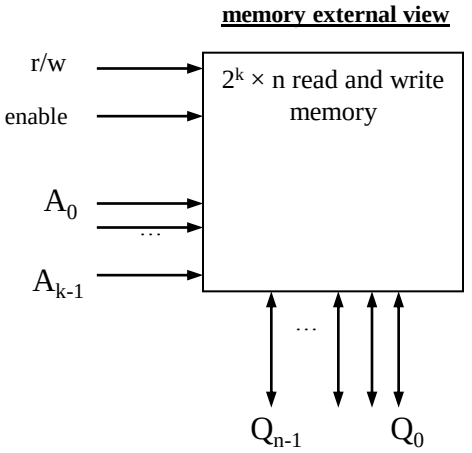
Data Alignment

- Data alignment
  - A datum with multiple bytes need to be allocated to an address that is a multiple of its size
- Examples
  - 0bxxxxxxxxxx byte (8bit) aligned
  - 0bxxxxxxxxx0 half word (16bit) aligned
  - 0bxxxxxxxx00 word (32bit) aligned
  - 0bxxxxxxx000 double word (64bit) aligned
- Why aligned?
  - Misalignment causes implementation complications and reduces performance

Memory device: basic concepts

- Stores large number of bits
  - *m* x *n*: *m* words of *n* bits each
  - k = $\text{Log}_2(m)$ address input signals
  - or *m* = 2^k words
  - e.g., 4,096 x 8 memory:
    - 32,768 bits
    - 12 address input signals
    - 8 input/output data signals
- Memory access
  - r/w: selects read or write
  - enable: read or write only when asserted
  - multiport: multiple accesses to different locations simultaneously





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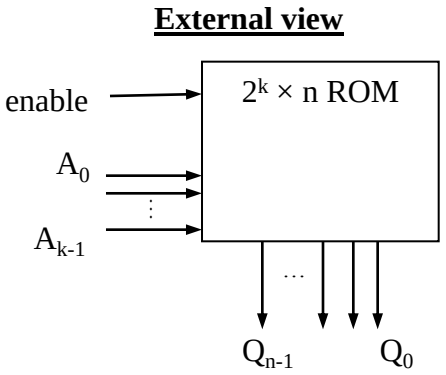
Memory Types

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

ROM: "Read-Only" Memory

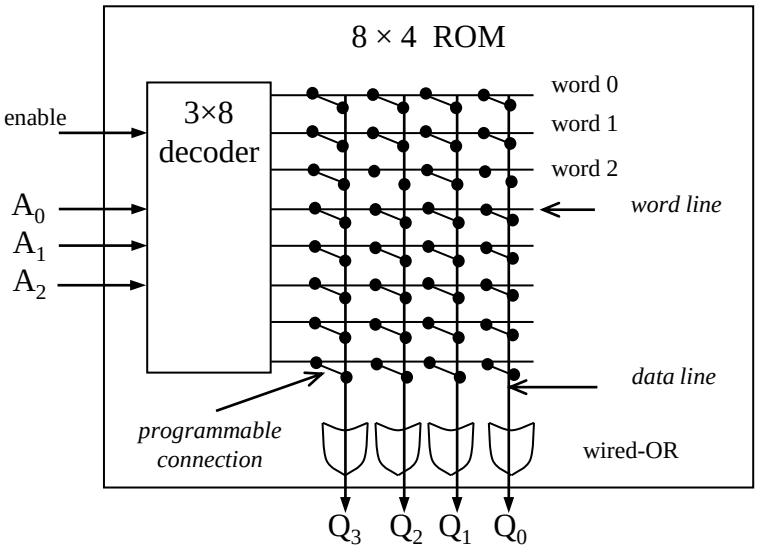
- Nonvolatile memory
- Can be read from but not written to, by a processor in an embedded system
- Traditionally written to, "programmed", before inserting to embedded system
- Uses
  - Store software program for general-purpose processor
    - program instructions can be one or more ROM words
  - Store constant data needed by system
  - Implement combinational circuit



Example: 8 x 4 ROM

- Horizontal lines = words
- Vertical lines = data
- Lines connected only at circles
- Decoder sets word 2's line to 1 if address input is 010
- Data lines Q_3 and Q_1 are set to 1 because there is a "programmed" connection with word 2's line
- Word 2 is not connected with data lines Q_2 and Q_0
- Output is 1010

Internal view

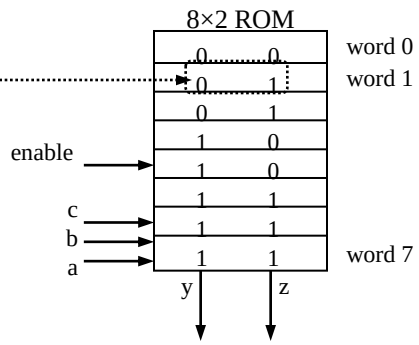


Implementing combinational function

- Any combinational circuit of *n* functions of same *k* variables can be done with 2^*k* x *n* ROM

Truth table

Inputs (address)			Outputs	
a	b	c	y	z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

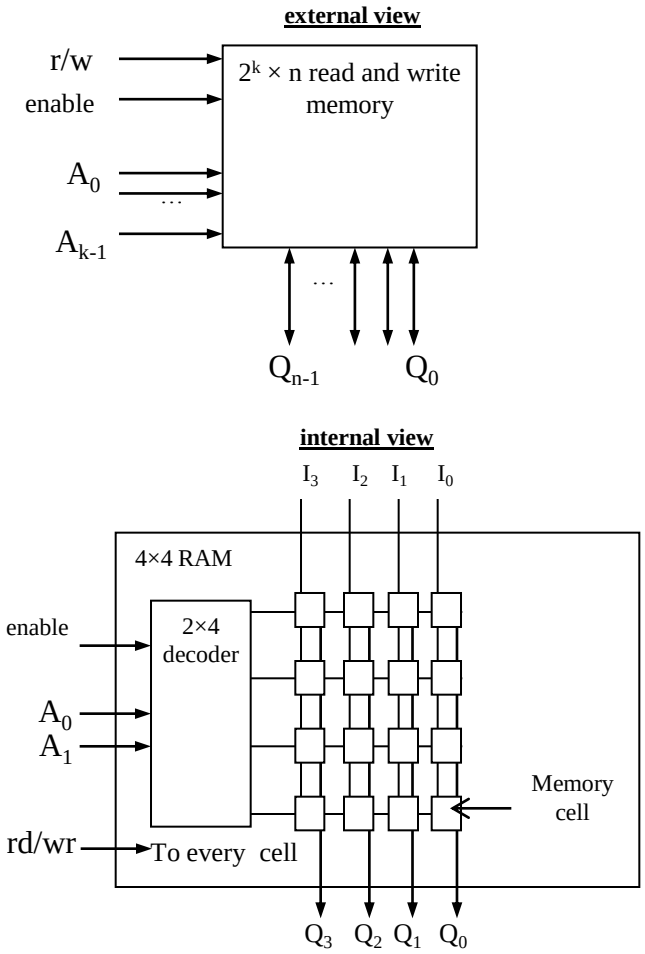


Types of ROM

- Written during manufacture
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read "mostly"
  - Erasable Programmable (EPROM)
    - Erased by UV
    - can program and erase individual words
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
    - can program and erase individual words as well
  - Flash memory
    - Large blocks of memory read/write at once, rather than one word at a time
    - Faster erase

RAM

- Random access memory
- Typically volatile memory
  - bits are not held without power supply
- Read and written easily by processor during execution
- Internal structure more complex than ROM
  - a word consists of several memory cells, each storing 1 bit
  - each input and output data line connects to each cell in its column
  - rd/wr connected to every cell
  - when row is enabled by decoder, each cell has logic that stores input data bit when rd/wr indicates write or outputs stored bit when rd/wr indicates read



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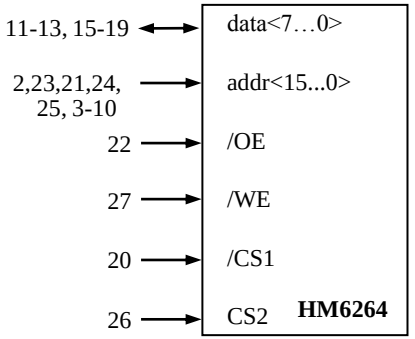
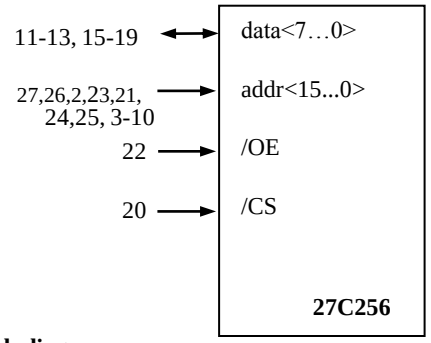
Types of RAM

- SRAM: Static RAM
  - Memory cell uses flip-flop to store bit
  - Holds data as long as power supplied
- DRAM: Dynamic RAM
  - Memory cell uses transistor and capacitor to store bit
  - More compact than SRAM
  - "Refresh" required due to capacitor leak
  - Slower to access than SRAM

Device Schematic and Time Diagram

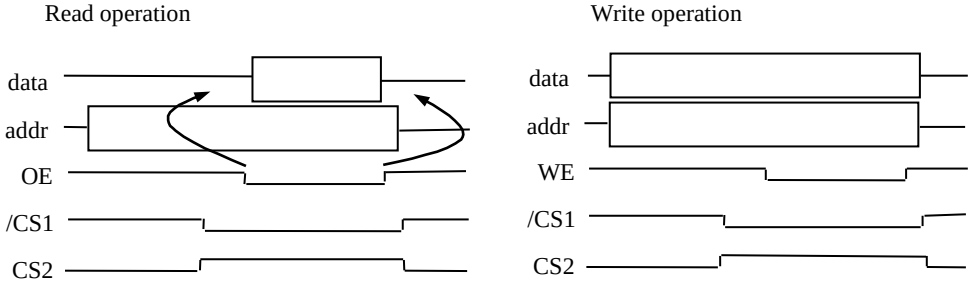




block diagrams

Device	Access Time (ns)	Standby Pwr. (mW)	Active Pwr. (mW)	Vcc Voltage (V)
HM6264	85-100	.01	15	5
27C256	90	.5	100	5

device characteristics



timing diagrams

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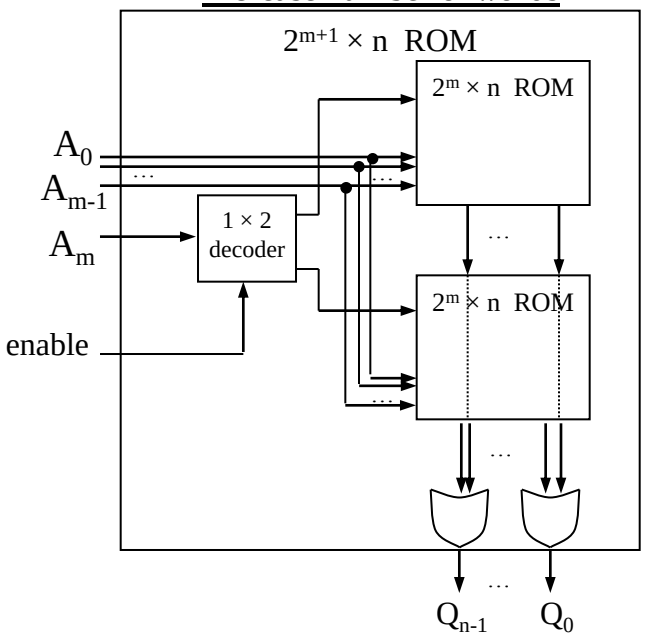
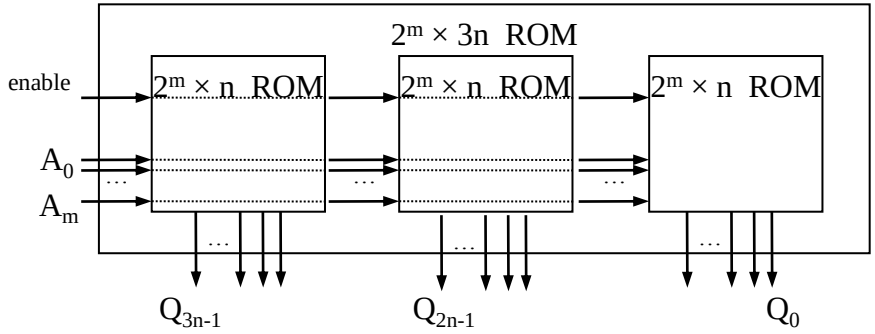
Composing memory

- Memory size needed often differs from size of readily available memories
- When available memory is larger, simply ignore unneeded high-order address bits and higher data lines
- When available memory is smaller, compose several smaller memories into one larger memory
  - Connect side-by-side to increase width of words
  - Connect top to bottom to increase number of words
    - added high-order address line selects smaller memory containing desired word using a decoder
  - Combine techniques to increase number and width of words

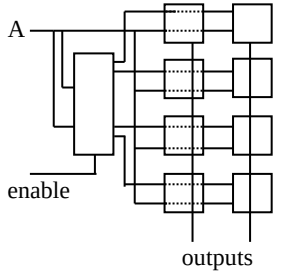
Increase number of words



Increase width of words



Increase number and width of words



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Summary

- Memory hierarchy
- Memory/processor architecture
- Memory access process
  - Endianness
  - Data alignment
- Memory data organization
- Memory devices
  - Basics
  - ROM/RAM