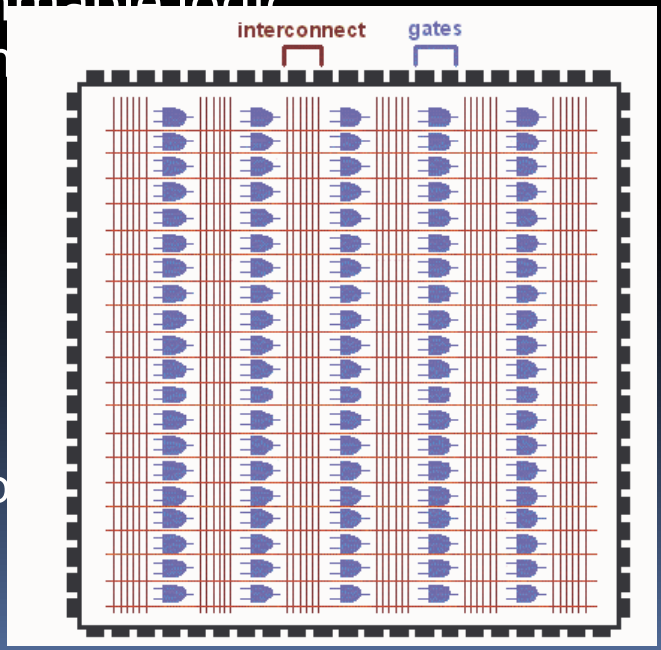
FPGA and Xilinx ISE

FPGA Basics

- What is FPGA
  - Field Programmable Gate Array
  - An FPGA is a regular structure of logic cells (modules) and interconnect, which is under the designer's complete control.
  - An FPGA is really some programmable logic with a whole bunch of programm
- How to program
  - Volatile
    - SRAM-Based, reprogrammable
  - Non volatile
    - Anti-fuse, one time programmab

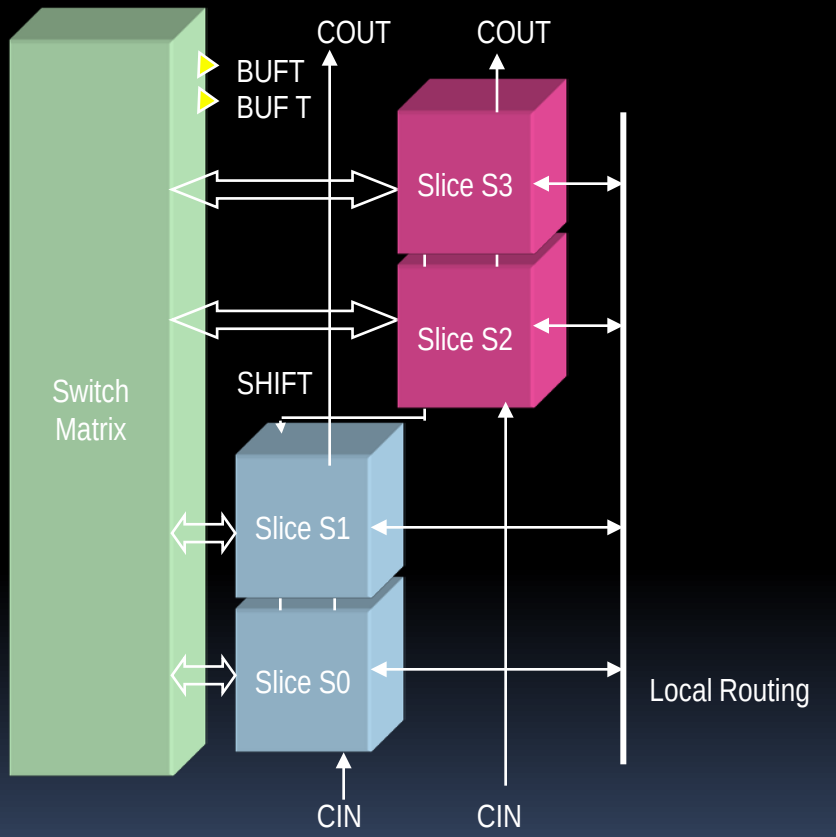


Inside FPGA

- All Xilinx FPGAs contain some basic resources
  - Slices (grouped into Configurable Logic Blocks (CLBs))
    - Contain combinatorial logic and register resources
  - IOBs
    - Interface between the FPGA and the outside world
  - Programmable interconnect
  - Other resources
    - Memory
    - Multipliers
    - Processors
    - Clock management

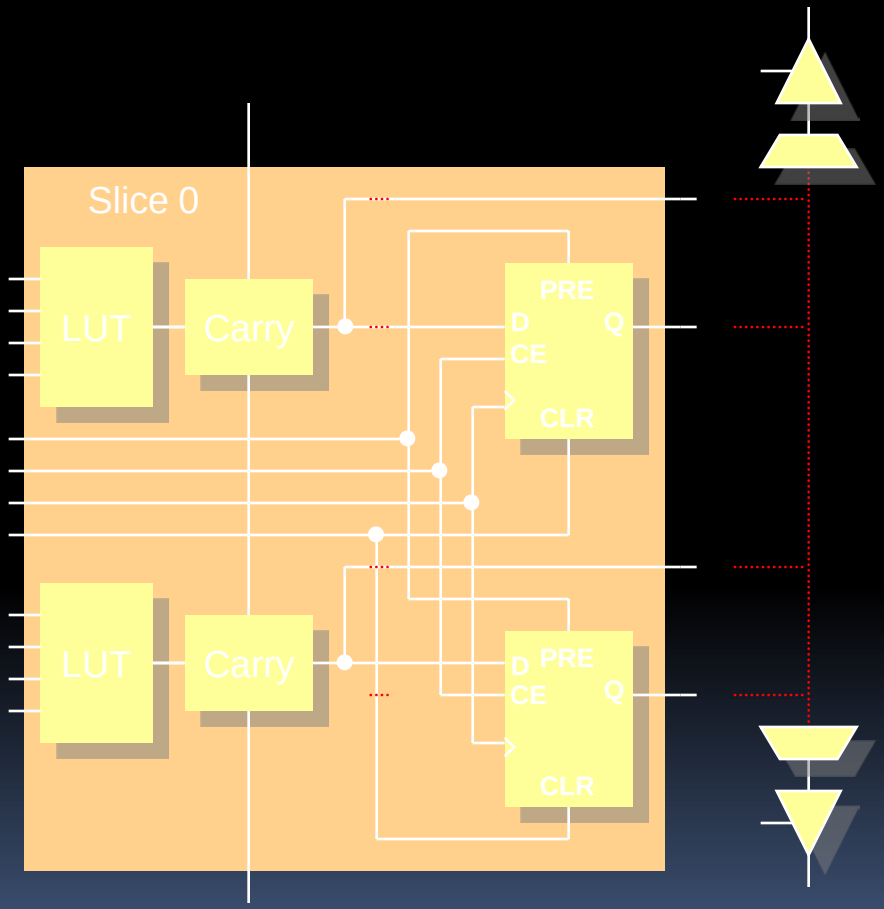
Slices and CLBs

- Each Virtex™-II CLB contains four slices
  - Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
  - A switch matrix provides access to general routing resources



Simplified Slice Structure

- Each slice has
  - Two 4-input look-up tables (LUTs)
    - Any 4-input logic functions
  - Four outputs
    - Two registered outputs, two non-registered outputs
  - Carry logic
    - Fast arithmetic logic
  - Other controls
    - e.g. set/reset



Virtex-II Pro Features

- Up to 24 RocketIO™ Multi-Gigabit Transceiver (MGT) blocks
  - Serializer and deserializer (SERDES)
  - Fibre Channel, Gigabit Ethernet, XAUI, Infiniband compliant transceivers, and others
  - 8-, 16-, and 32-bit selectable FPGA interface
  - 8B/10B encoder and decoder
- PowerPC™ RISC processor blocks
  - Thirty-two 32-bit General Purpose Registers (GPRs)
  - Low power consumption: 0.9mW/MHz
  - IBM CoreConnect bus architecture support

VIrtex-II-Pro Datasheet

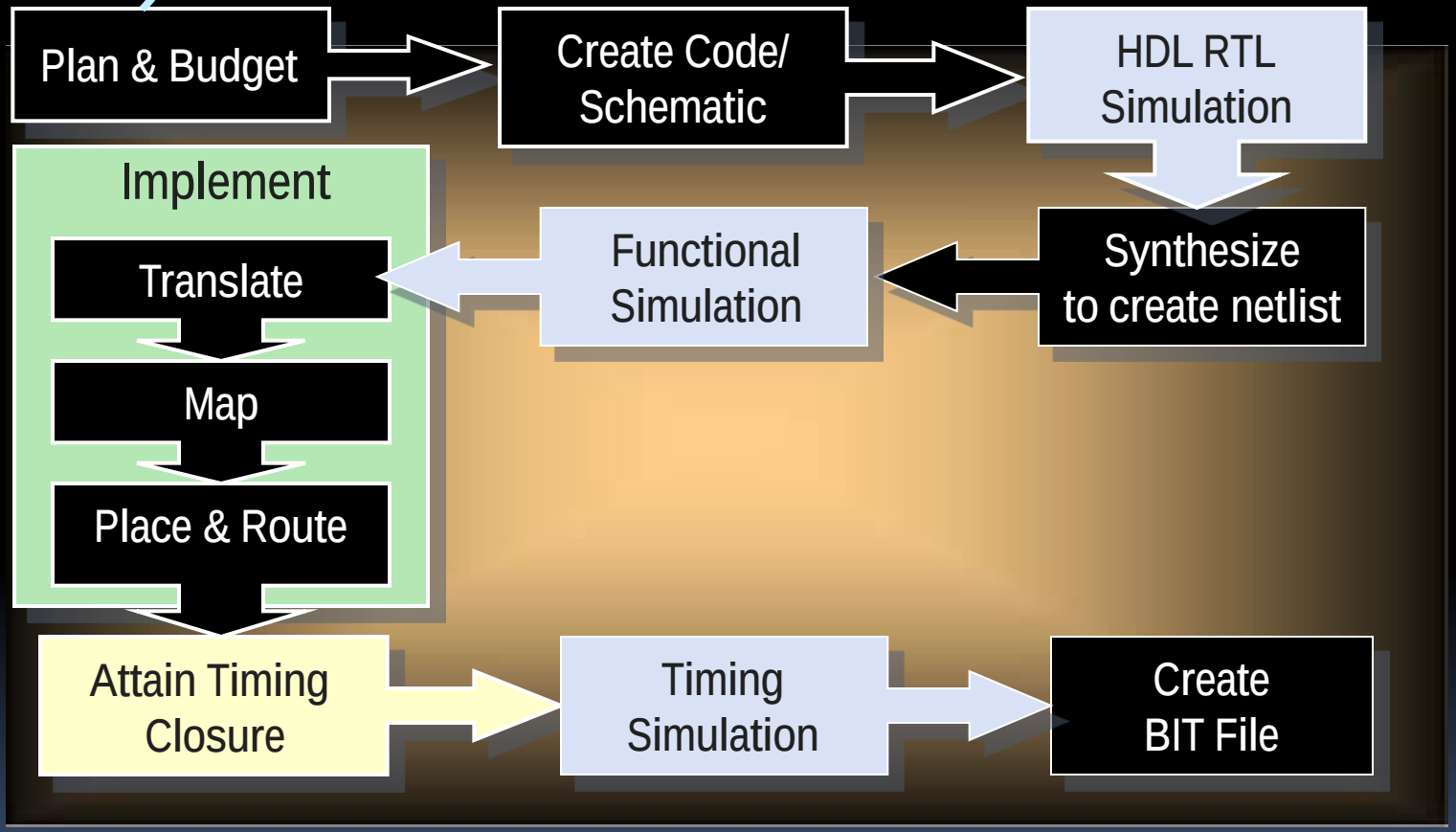
Table 1: **Virtex-II Pro / Virtex-II Pro X FPGA Family Members**

Device[1]	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells[2]	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8[4]	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0[3], 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0[3] or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20[4]	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0[3] or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

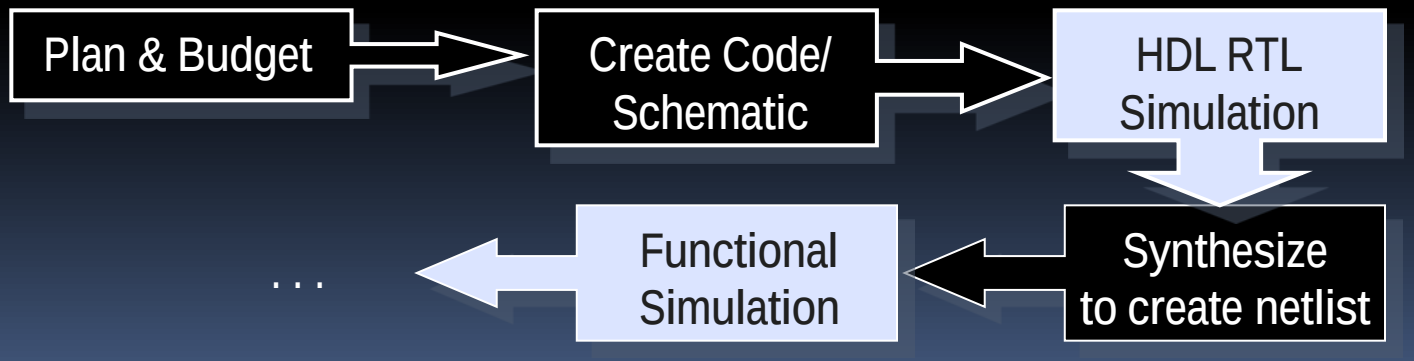
1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

FPGA Design Flow (Xilinx ISE)



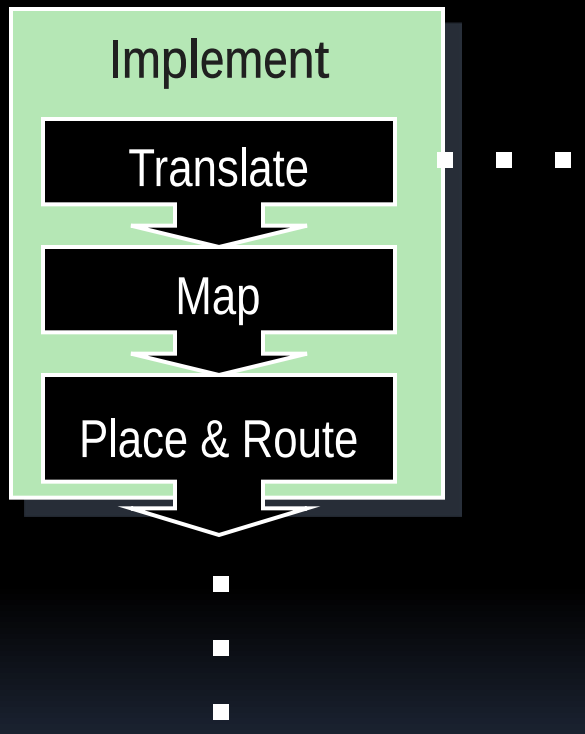
Design Entry

- Plan and budget
- Two design-entry methods: HDL or schematic
- Whichever method you use, you will need a tool to generate a netlist for implementation
  - Netlist: A text file that describes the actual circuit to be implemented at very low (gate) level
- Simulate the design to ensure that it works as expected!



Xilinx Implementation

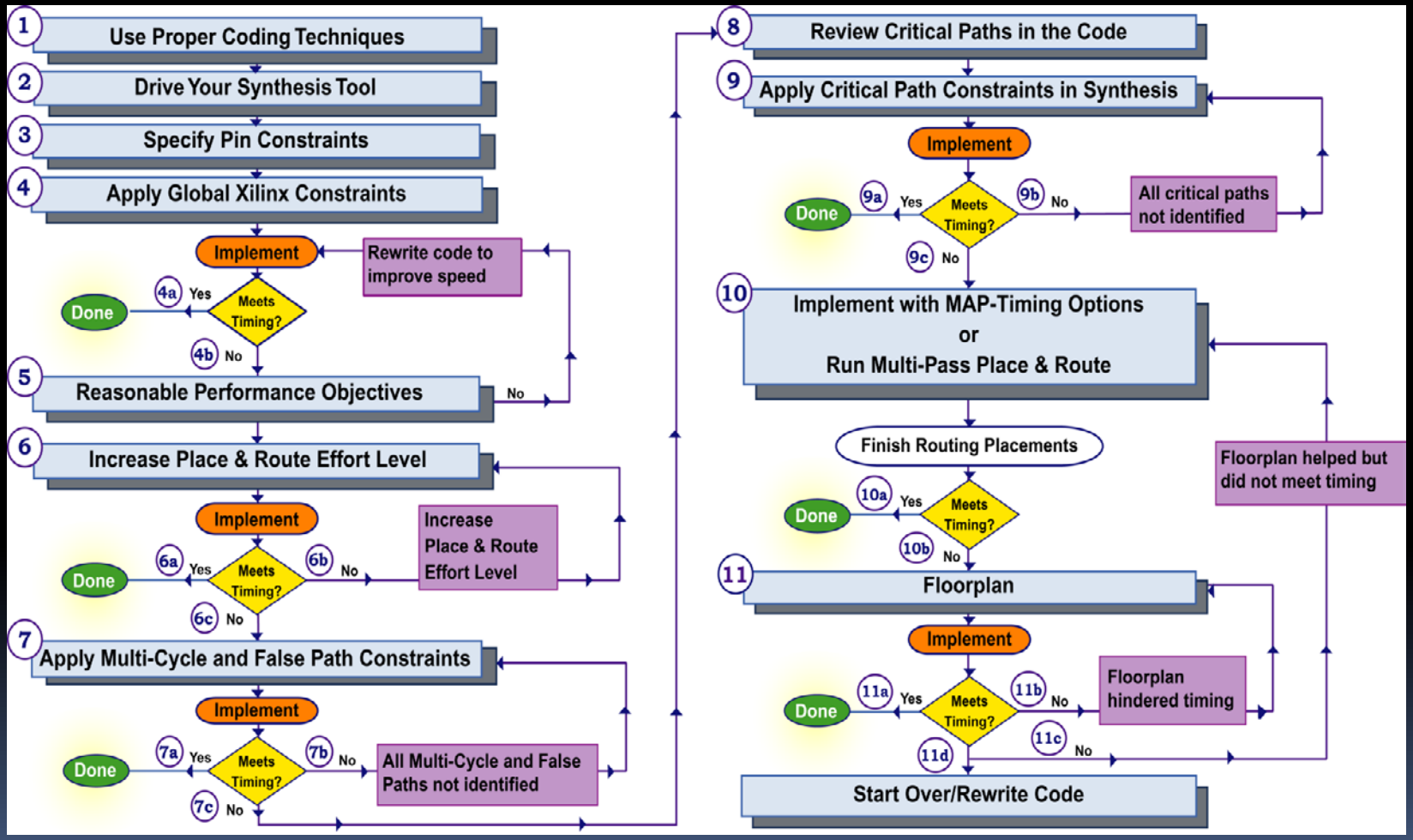
- Once you generate a netlist,
  you can implement the design
- There are several outputs of implementation
  - Reports
  - Timing simulation netlists
  - Floorplan files
  - FPGA Editor files
  - and more!



What is Implementation?

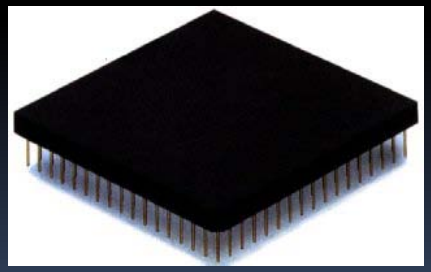
- Implementation includes many phases
  - **Translate:** Merge multiple design files into a single netlist
  - **Map:** Group logical symbols from the netlist (gates) into physical components (slices and IOBs)
  - **Place & Route:** Place components onto the chip, connect the components, and extract timing data into reports
- Each phase generates files that allow you to use other Xilinx tools
  - Floorplanner, FPGA Editor, XPower

Timing Closure



Download

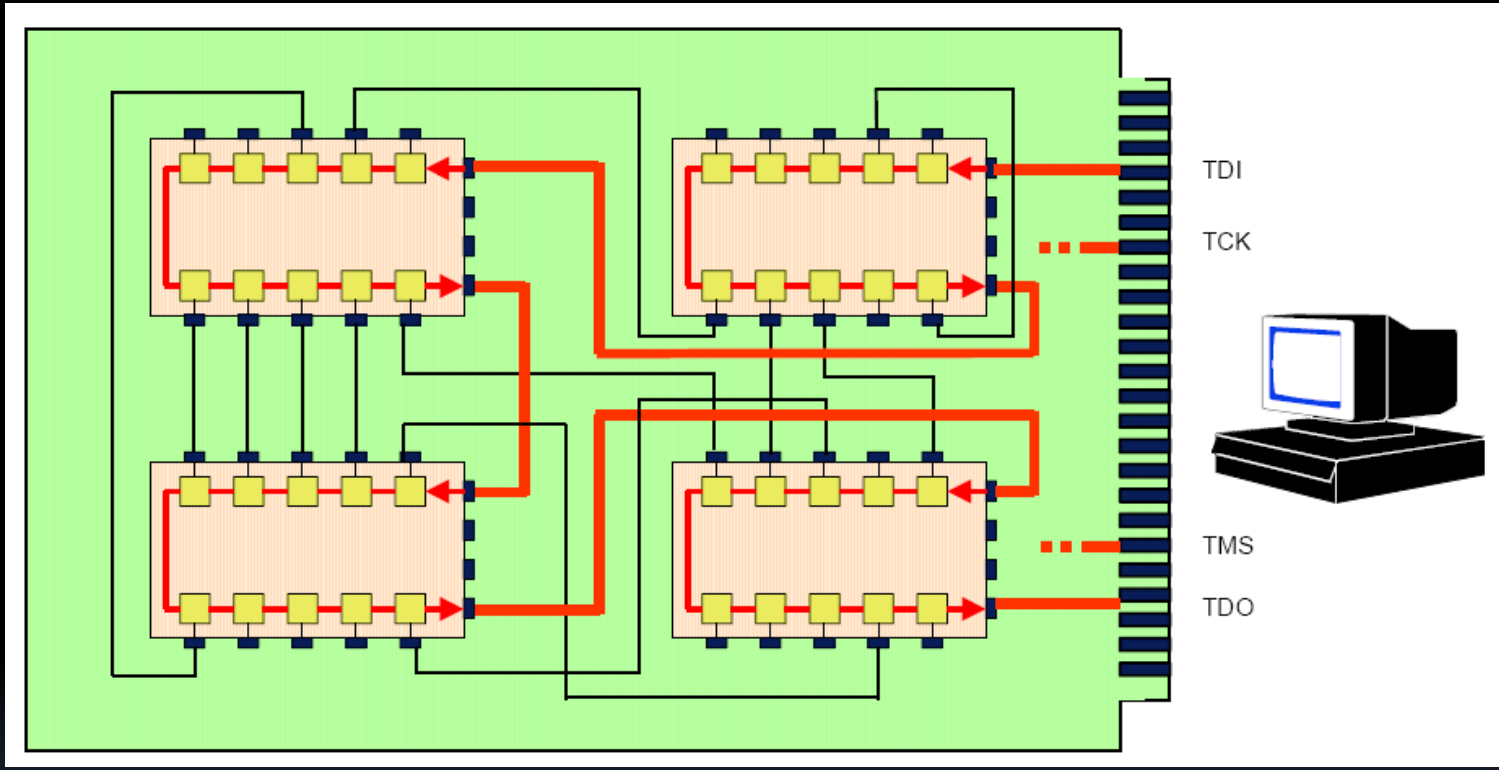
- Once a design is implemented, you must create a file that the FPGA can understand
  - This file is called a bitstream: a BIT file (.bit extension)
- The BIT file can be downloaded directly into the FPGA, or the BIT file can be converted into a PROM file, which stores the p information



JTAG and Boundary Scan Technology

- In the 1980s, the *Joint Test Action Group* (**JTAG**) developed a specification for boundary-scan testing that was standardized in 1990 as the IEEE Std 1149.1, and later revised in 1993 (titled 1149.1a).
- Boundary-scan architecture
  - Each boundary-scan cell including a multiplexer and latches is assigned to each pin on the device
  - Boundary-scan cells can capture data from pin or core logic signals, or force data onto pints.
    - The captured data is serially shifted out and externally compared to the expected results
    - Forced data is serially shifted into the boundary-scan cells
  - Boundary-scan cells form a serial data path called the ***scan path*** or ***scan chain***.

Boundary Scan



To know more details: **Boundary Scan Tutorial, http://www.asset-intertech.com/pdfs/boundaryscan_tutorial.pdf**