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Custom Software Simulation Tool for CMOS Technology

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1 Introduction

Simulation is about building and exercising the model of a system that is being designed. One of the key objectives of the simulation is to verify the functional correctness of the system. In the electrical domain, simulation is a means of validating an electronic circuit, whether a digital circuit, an analog circuit or both. By digital circuits it's referred to those circuits that use discrete logic levels('0','1','X',etc.) for all the data manipulations. By analog circuits it's referred to those circuits that make use of the properties of continuous-time electrical components such as resistors and capacitors to describe the behavior of a circuit. The advancements in VLSI design technology have caused current systems to be a combination of both analog and digital sub-systems, rather than being isolated digital and analog systems. The lack of user friendly tools that allow the unexperienced person to be gradually introduced to VLSI world make that person have isolated ideas about the particular behavior of the CMOS components but it is still difficult to have a large picture of the whole. This project focuses on digital simulation as an essential component of better understanding of parameters relationship when CMOS circuits are designed.

Simulation is one of the essential *Computer-Aided-Design(CAD)* tools used in the *Electronic Design Automation(EDA)* industry today, to achieve a wide variety of goals, quickly and efficiently. To achieve these goals, the simulation process requires three sets of data and a program:

- A means to describe the system to be simulated (Language).
- A description of the system to be simulated (Model).
- A description of the inputs to the model (Test Bench).

- A mechanism to process the above in a manner that mimics or simulates the system being designed (Simulator).

To exploit the expressiveness of a language and to evaluate the performance of a simulator, it is necessary to build appropriate models and suitable test-benches. This has been a key factor that motivated our project, which represents the semiconductor device models in a visual basic program. Simulation is chosen as a means to validate these models as it is one of the easiest and the most appropriate techniques practiced today to validate a model. Models provided by earlier works are validated using the visual basic program.

2 Modeling

As mentioned above, one of the elemental prerequisites for simulation is a model. A model of a system is a representation of its behavior in a form which the simulator can understand and process. *Model fidelity*, how close the model is to the actual system being designed, is an important criterion in modeling a system. *Model accuracy*, how close the representation of the model is to an ideal system, is another important criterion to be considered while characterizing a system. Writing accurate models is a difficult and skilled task, but how accurate we want the model to be is determined by the purpose of the model.

There are different ways to model the behavior of a system. Models can be discrete-event, continuous-time or both, in a way that is understood by a particular simulator. Two of the many ways to represent a discrete-time model are: 1) by means of communicating

processes with discrete-event signals as information carriers or 2) by means of boolean equations. One of the many ways to represent a continuous-time models is by means of analytical or mathematical equations. Semiconductor Device models performed in this project fall into the category of continuous-time(analog) models.

2.1 Levels of Modeling

There are different levels of abstraction at which parts of a design can be modeled. The level of abstraction at which the model is to be represented is determined by the purpose of the model. Traditionally, the primary purpose of the model is to verify the functional correctness of a design. However, should be noticed that the main purpose of this work is to develop a friendly tool that allow people to easily understand the processes achieved inside the CMOS technology. To better explain the levels of abstraction a simple NAND function is taken into consideration.

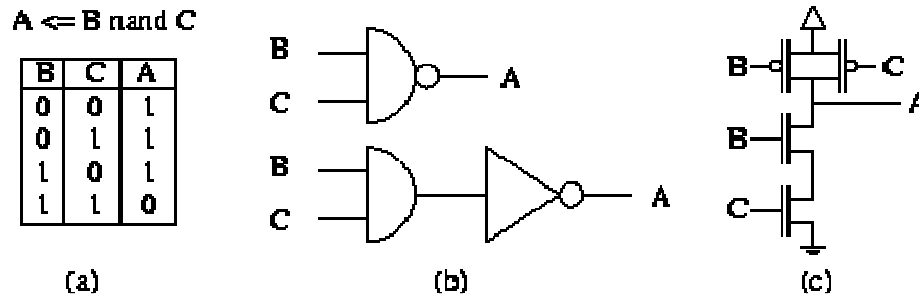


Figure 1 MOS transistor inverter schematic

- **High Level :** This level is also referred to as behavioral level. This is a level of description equivalent to the high-level procedure in programming. The function is described in terms of addition, subtraction, division etc or simple boolean

equations. As an example a NAND function may be represented as a boolean equation or a table, as shown in figure1(a).

- **Gate Level** : This level of description uses simple logic gates as the basic elements of the model. The logic elements may include multiplexers, flip-flops etc., which in-turn are described at behavioral level using boolean equations. At this level the purpose of the model is not restricted to functional verification, it may be used to verify the timing constraints of the design too. As an example the NAND function may be represented as shown in figure1(b).
- **Switch Level** : Switch level representation is a trade off, in terms of speed and accuracy, between gate level and circuit level. At this level of model description transistors are treated as simple switches that are either open or closed. Timing may be included in switch level simulation. As an example the NAND function can be represented as shown in figure1(c), replacing transistors with simple switches, which are either open or closed depending on the inputs.

All the models presented in this project fall into the category of switch level modeling.

2.2 Equivalent-Circuit Device Model

The characterization of semiconductor devices requires a suitable means of describing their physical and electrical properties. The model can be derived from theoretical considerations or from an empirical approach. In the former case the circuit elements may be chosen to represent physical attributes of the device. This project discuss two different ways to characterize the physical and electrical properties of semiconductor devices. Semiconductor device models can be broadly divided into *physical device* models and

equivalent-circuit models. Physical models can be used to predict both terminal characteristics and transport phenomena, whereas equivalent-circuit models are restricted to an electrical description of the device characteristics, although it is possible in many cases to relate these characteristics to the device physics.

Equivalent circuit models are based on the electrical characteristics of the device that are based on the association of electrical circuit elements with the device structure. Equivalent circuit models can be considered as a trade off between completely physical and completely analytical models. This class of models uses a little of device physics to relate the dimensions of the device to the electrical properties of the device and transform the carrier transport equations of the device into closed loop analytical equations, which can be solved much much easy and faster as compared to the carrier transport equations of the device. Despite the ease with which many equivalent circuit models can be evaluated, equivalent circuit modeling techniques have some important limitations. At higher frequencies the models become increasingly more complex and it is difficult to equate the model elements values with the physical parameters of the device (although a qualitative identity still exists). Furthermore, since the element values are dependent on bias, signal level and frequency, the models become increasingly non-linear with signal level and frequency. There have been many attempts to account for these phenomena in the models but it is difficult to obtain accurate large-signal models for existing devices.

The equivalent-circuit models are strongly dependent on frequency, DC bias, signal level and temperature. It is convenient to divide the equivalent circuit models into DC and AC models. At higher frequencies these models may also be sensitive to the impedance of the

embedding circuit, hence it is generally necessary to discriminate between *small-signal* and *large-signal* models. This thesis mainly focuses on static(DC) and large-signal equivalent-circuit models. Static means those models which can operate at low frequencies(below 1 kHz) and at DC, irrespective of the signal level. By large-signal we refer to those models which can operate at high frequencies (above 1 kHz), taking into account the impedance of the embedding circuit. These models are sometimes referred to as charge-storage models, as they have finite switching times that are greater than zero. Large signal models, as the name suggests, can operate under large variations of the input signal.

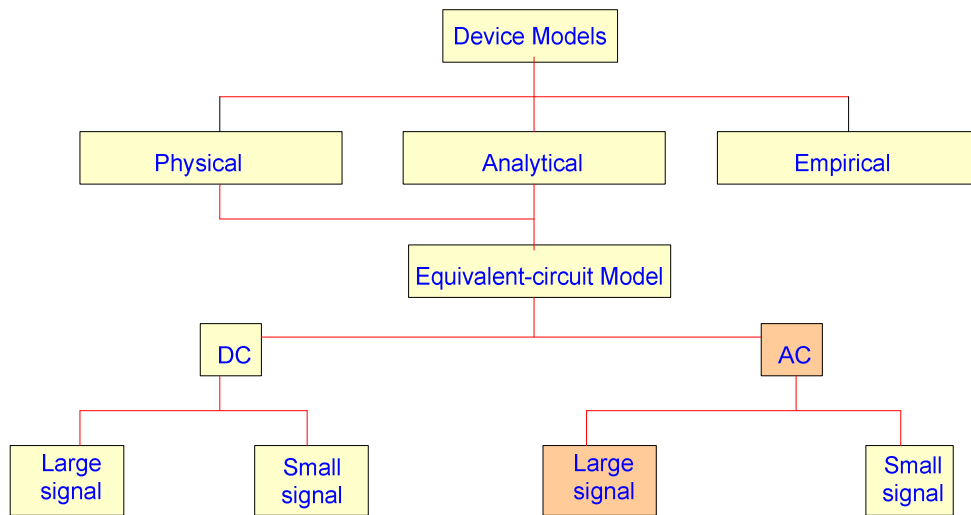


Figure 2 MOSFET Model characteristic

2.3 Spice Models

The initial models written for SPICE were very elemental and could capture only limited properties of the semiconductor devices. Later these elemental models were used to

develop more and more complex models which can characterize most of the physical and electrical properties of the semiconductor devices.

These models are clearly based on the original intention of a physically based analytical FET model, with all geometry dependent included in the model equation. The first generation of models is comprised of :

- **LEVEL 1** : This model is sometimes referred to as "Shichman-Hodges" model. Simplifications such as gradual channel approximation and the square law for the saturated drain current are employed. Channel length modulation, was the only geometry effect and no sub-threshold conduction model is included.
- **LEVEL 2** : This model includes the more detailed description of depletion region, the threshold region and the mobility reduction by the vertical field. A model for the reduction of the saturation voltage by the velocity saturation is included. A sub-threshold current model is also introduced for the first time.
- **LEVEL 3** : This model was developed to overcome the observed shortcomings of Level 2 model. Level 3 takes the semi-empirical approach, which places more emphasis on parameter extraction, while the structure is basically similar to Level 2. The basic difference between Level 2 and 3 is that Level 3 model is more efficient mathematically, and at least accurate as Level 2.

The second generation of models, the equations are subject to extensive mathematical conditioning, with a clear focus on their circuit simulation usage. In addition to empirical inclusion of the device geometry in the basic model equations, an entirely separate

parameter structure is created solely to describe the geometry dependence. This generation of models is comprised of :

- **BSIM1** : In this model structure, the emphasis is clearly on the mathematical conditioning for circuit simulation. The approach to the description of small geometry effects is strict. This includes improved (although empirical) descriptions of the threshold voltage and the mobility; in addition, a more detailed sub-threshold current model is introduced. Overall, BSIM1 is an improved digital model.
- **BSIM2** : BSIM 2 is closely based on BSIM 1. It employs several expressions developed from two dimensional analysis, and makes extensive modifications to the BSIM description of the mobility and the drain current, including a new sub-threshold current model. An output conductance model is added, making BSIM2 suitable for analog circuit design.
- **HSPICE Level 28** : This is a proprietary model developed by Meta-Software. Through extensive mathematical conditioning, HSPICE Level 28 has been made suitable for analog design. A unique feature of HSPICE Level 28 is that the model structure is designed to accommodate model binning. However, the model parameter set is almost entirely empirical.

3 MOSFET Model

Metal Oxide Semiconductor Field Effect Transistor(MOSFET) is a four-terminal device consisting of source(S), drain(D), gate(G) and the substrate(B). Unlike the JFET where the gate is electrically connected to the source and the drain, the MOSFET gate is

insulated from the source and the drain, hence the MOSFET is sometimes referred to as Insulated-Gate Field-Effect Transistor(IGFET). MOSFET structure has two possible configurations: *n-channel* and *p-channel*, which is determined by the substrate over which the device is fabricated. An *n-channel* MOSFET (n-MOS) is made of a *p-type substrate* on which a layer of thermal-oxide is built. A high concentration of *n-type* dopant is thermally diffused inside the silicon to obtain so-called *source* and *drain* . On the thin-oxide layer a conducting material is deposited, which acts as a *gate*. The region covered by the thin-oxide layer and by the gate represents the *channel*. A *p-channel* MOSFET (p-mos) is also fabricated in a similar fashion, by using an *n-type substrate* and a *p-type* dopant.

A MOS transistor is termed a majority-carrier device, in which the current in a conducting channel between source and the drain is modulated by a voltage applied to the gate. The normal conduction characteristics of an MOS transistor can be divided into three regions of operation based on the voltages, as shown below:

- **Cut-off region:** where the current flow is essentially zero.
- **Non-saturated (Linear) region:** weak inversion region where the drain current is dependent on the gate and the drain voltage, with respect to the substrate.
- **Saturated region:** channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage(strong inversion region).



Figure 3. PMOS structure

This project regards the static and large-signal models of a *n-channel* MOSFET, the *p-channel* MOSFET models can be obtained by appropriately reversing the direction of junction voltages and currents.

3.1 Model Equations

This particular desing tool relays aon the theory and basic equations found in the CMOS technology. Most of the parameters required for modelling have been extracted form the class book.

3.1.1 Input Parameters

- Type: NMOS or PMOS
- T (temperature) optional
- Gate oxide thickness t_{ox} (range 2-20 nm)
- Doping N (range 1.1×10^{14} thru $9.99 \times 10^{17} / \text{cm}^3$)
- Total transistor length TL (range 1-10 μm)

- Channel length L (range 1-4 μm)
- Channel width W (range 1-20 μm)

3.1.2 Calculated Parameters

- Mobility $\mu = \mu_1 + \frac{\mu_2 - \mu_1}{1 + \left(\frac{N}{N_{ref}}\right)^\alpha}$ Equation [3.33]
- Capacitance $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_0}{t_{ox}}$ Equation [6.23] Page 202
- Process transconductance $\kappa' = \mu C_{0x}$ Equation [6.22] Page 202
- Transconductance $\beta = \kappa' \left(\frac{W}{L}\right)$ Equation [6.21] Page 202
- Bulk Fermi Potential $|\phi_F| = \left(\frac{kT}{q}\right) \ln\left(\frac{N}{n_i}\right) \cong 0.02585 \ln\left(\frac{N}{n_i}\right)$ [6.14] Pg.197
- Threshold voltage $V_{th} = \frac{1}{C_{0x}} \sqrt{2q\epsilon_{Si} N (2|\phi_F|)} + 2|\phi_F|$ Eq. [6.16] Pg. 197
- FET ON resistance $R = \frac{1}{\beta(V_{DD} - V_{th})}$ Eq. [6.73] Page 215
- Drain (or Source) Capacitance $C_D = \frac{1}{2} C_{0x} LW + C_j A + C_{jsw} P$ [7.29] Pg. 246
- Total nFET+pFET output Capacitance $C_{FET} = C_{Dn} + C_{Dp}$ [7.33] Pg. 247
- Total inverter capacitance $C_{out} = C_{FET} + C_{LOAD}$ [7.32] Pg. 247
- Time constant nFET $\tau_n = R_n C_{out}$ [7.44] Pg. 249
- Time constant pFET $\tau_p = R_p C_{out}$ [7.52] Pg. 250
- Fall time $t_f = 2.2\tau_n$ [7.48] Pg. 250
- Rise time $t_r = 2.2\tau_p$ [7.54] Pg. 251
- Maximum frequency $f_{max} = \frac{1}{t_r + t_f}$ [7.55] Pg. 251

4 Software Implementation

The main purpose of this design software is to present a extremely friendly tools to guide the user through the most basic concepts behind the CMOS technology and allow to present interactive results of the related parameters when some modifications are performed to the basic paramenters driving this technology. As previously mentioned, the software design tool has been designed in a friendly enviroment (visual basic) which allows to present graphic results . The model used for the simulation process is the most basic one and it is described by the set of equations presented previuosly.

Three main windows allow acces to these three different components : NMOS component, PMOS component and TEST and MEASUREMENT component. Figure gives an overview of described components. As can be seen, these three windows show different fields that can be visualized as inputs or outputs according to the parameters described. For obvious reasons the program allows to change the inputs values but does not allow to change the output ones. Input paramenters can be modified by typing the desired valued in the corresponding field or alternatively, it can be changed by the modifying the corresponding slider.

According to the most basic CMOS tecnology fundamentals, total length, Channel length, Channel width, Oxide layer thickness, doping density, threshold voltage and supply voltage have been chosen as the input fabrication parameters to design an evaluate the logic function under test.

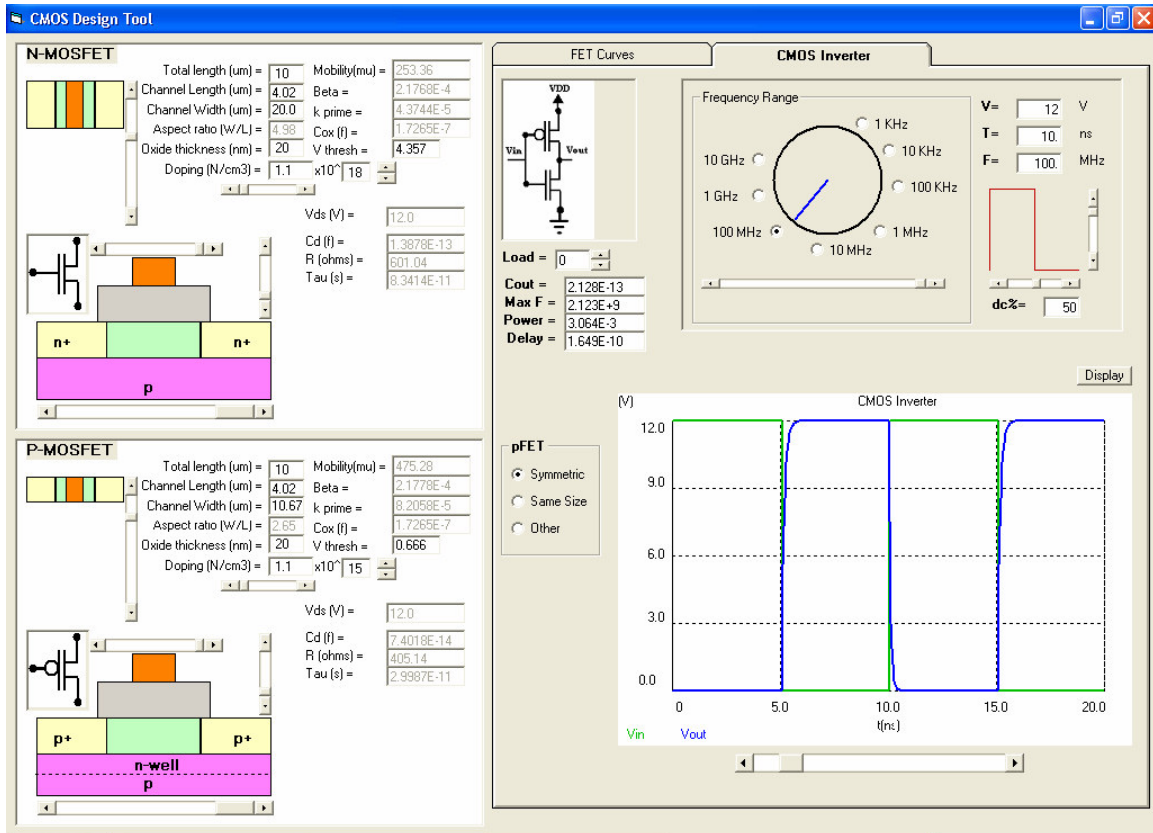


Figure 4. Software Design Tool main windows

All the output values are calculated and returned into the corresponding fields according to the input parameters configuration. One of the main purposes of this tools is letting the user know about the physical changes produced in the most basic structures (NMOS and PMOS) so, mimics of top and sides views are present to return information about these physical parameters when an input value is modified. All parameters (input and output) consider the corresponding units and the numerical values are between the normal limits that are used in current applications. Figure 2, 3 display the changes in channel length and oxide thickness for the NMOS transistor.

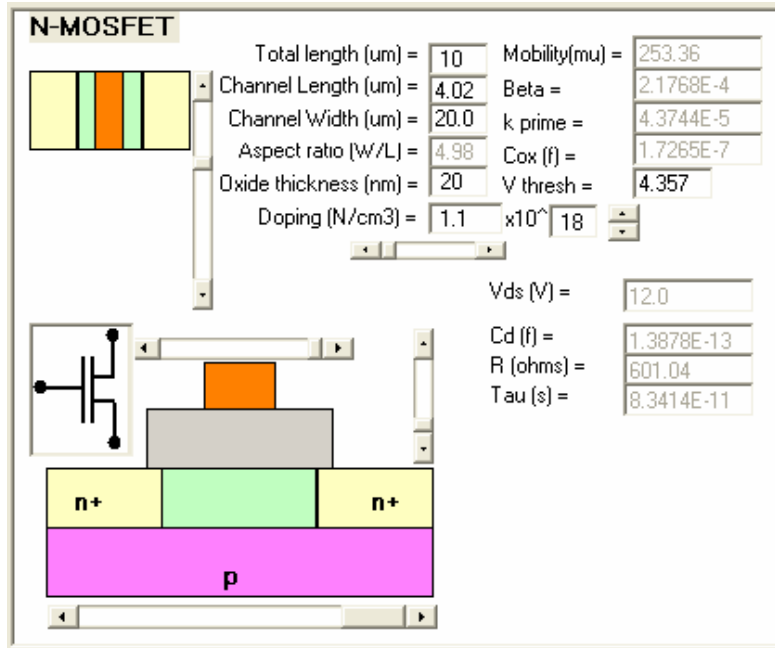


Figure 5. NMOS window

In addition to the graphical changes produced on the physical NMOS dimensions, all different output parameters have been recalculated in accordance.

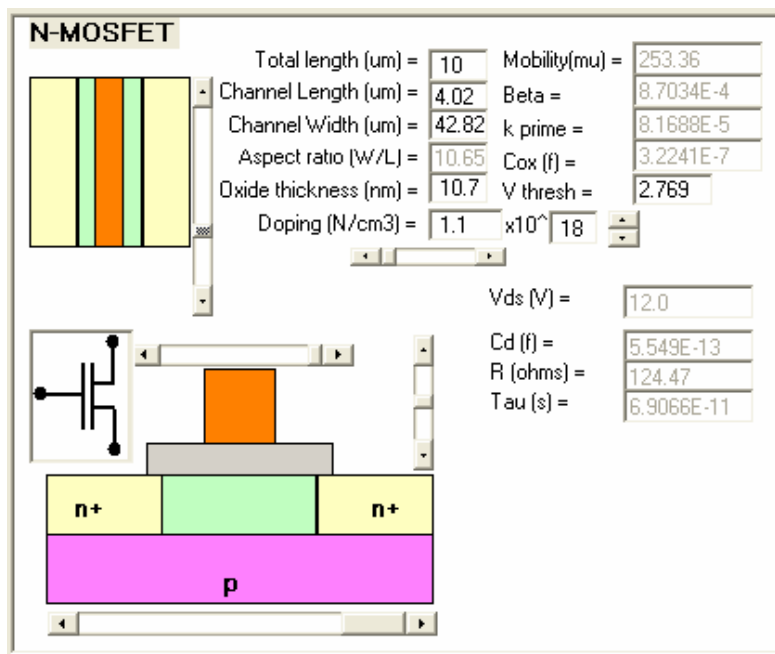


Figure 6. Adjusted NMOS window

The PMOS window is basically the same as NMOS window except that different input values corresponds to its physical structure. All parameters associated with this structure can be modified as desired in the same fashion as done with the NMOS structure.

One of the interesting features of this design tools is the ability to provide three different scenarios when a CMOS structure is been designed. The first one allows the user to setup input parameters for one of the NMOS and the program will design automatically the corresponding parameters for the PMOS structure that matches the symmetry criteria. Remember that NMOS and PMOS characteristic does not perform symmetrically respect to the rise and fall times.

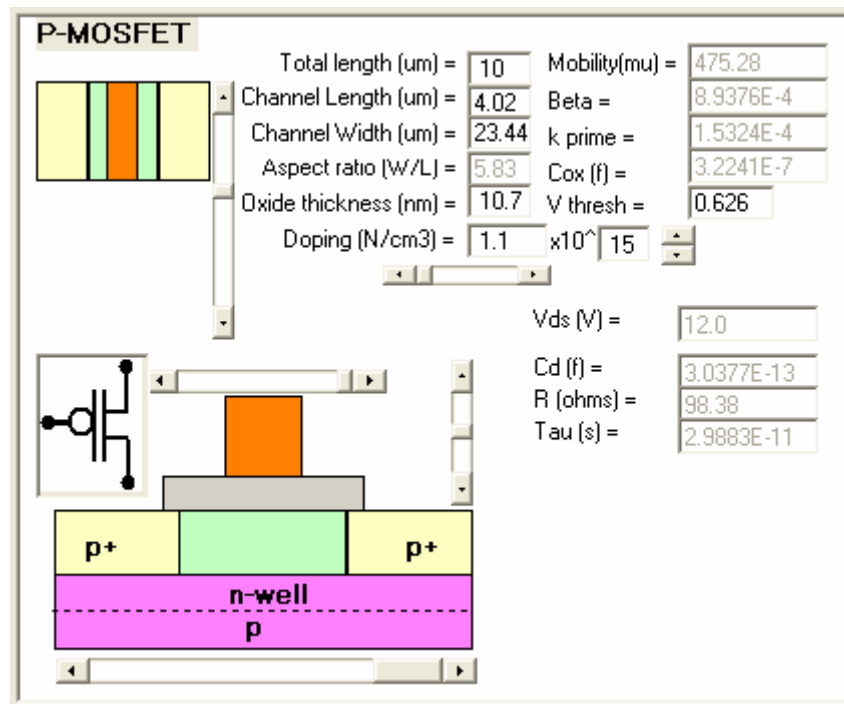


Figure 7. PMOS window

The second scenario is when the user wants to design for the same size for NMOS and PMOS structures. This is the case when least area criteria is having in mind. Remember that symmetry will not be allowed for this case.

The thir scenario is the most general one when the two structures can be defined independently and the same size or symmetry criteria is not the main objective during the design process. The desired selection requires to click on the selected field at the MEASUREMENT window.

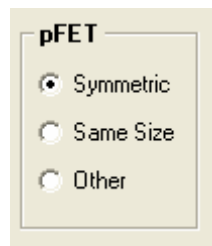


Figure 8. Selection Criteria

The third main window defines the input signal and the visualizing tools required to observe the output performance of the device under test (DUT). This window offers 3 main features to the user. The first one is the type of input signal driving the DUT which for this version is a square wave with full control of the most basic paramteres. The frequency range is between 1 kHz and 10 GHz with a continuos Duty Cycle selectrion between 0 and 100 %. Once again, the numercal values can be typed on the corresponding fields or alternatively, they can be extracted from the corresponding sliders. Should be noticed that the amplitud value selected for this input waveform also represent the Vds value required on the PMOS and NMOS structures. Figure 4 depicts the main controls on the function generator.

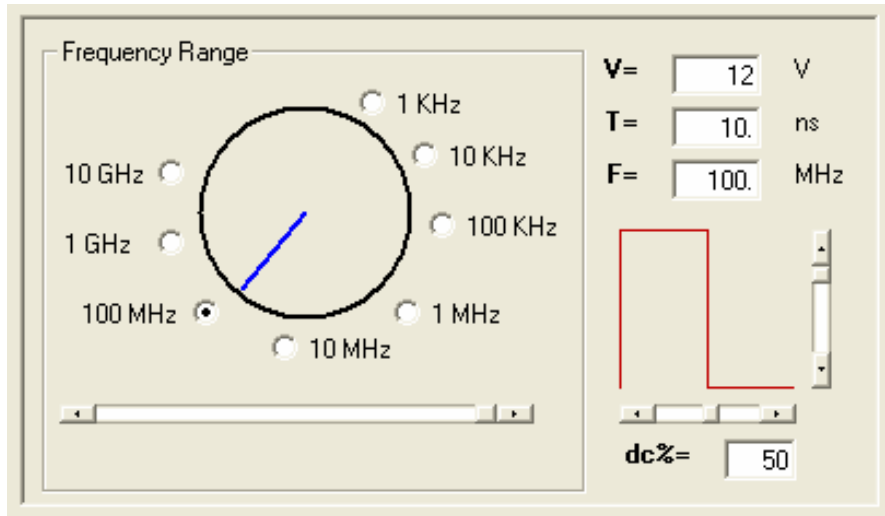


Figure 9. Virtual Function Generator.

The second main feature of the MEASUREMENT window is the DUT. This first version has been designed to support the typical inverter configuration. This feature allows to add fan out capability to the DUT to check for performance.

AS a result of this fanout capability , automatic result are generated in terms the total load capacitance, the power consumed the ideal maximum frequency would support this DUT and the output delay provided by it. Figure 5 illustrate the performance results.

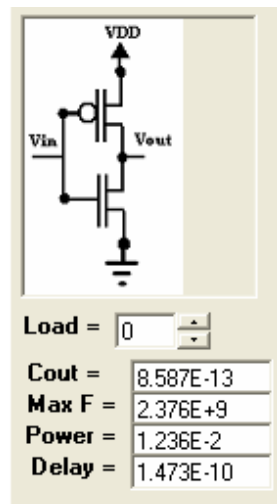


Figure 10. Performance paramters

The third main function corresponds to the output performance visualization using a virtual oscilloscope. Input and output signals (V_{in} and V_{out}) are represented in time domain according to the color code shown (Green and Blue correspondingly). The time scale is automatically adjusted according to the input frequency but further scale manipulations (zoom in or zoom out) can be performed by the corresponding scale slider. Figure 6 depicts the input and out signal from the inverter configuration according to the parameters previously chosen in this particular design.

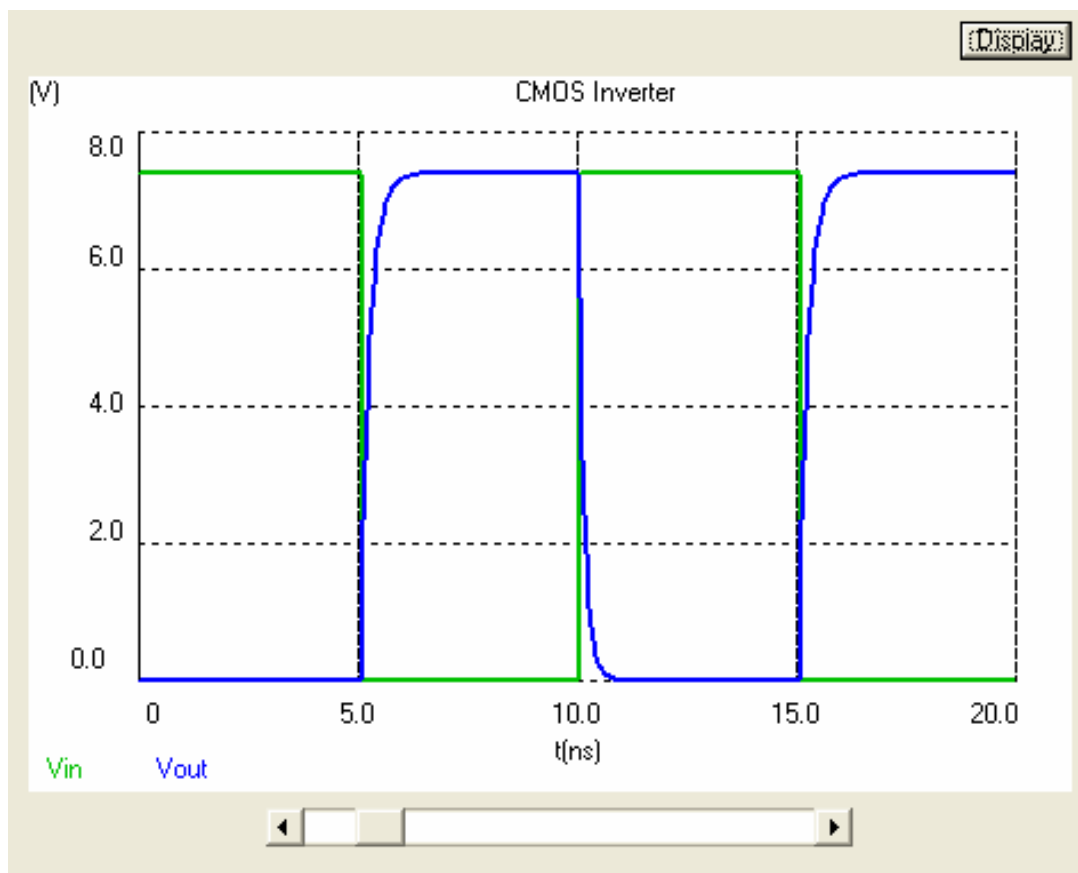


Figure 11. Visualization tool

As an extension of this MEASUREMENT window, there is a taped window that will show the corresponding MOSFET characteristic curves according to the input parameters used in the design process. This plot will show the relationship between the drain current (I_{ds}) as a function of the Drain-source voltage (V_{ds}) for several Gate-source voltages (V_{gs}). This is an easy illustration of the different MOSFET regions at which can be operate according to the input and bias conditions. Figure 7 depicts this relationship for the actual NMOS configuration.

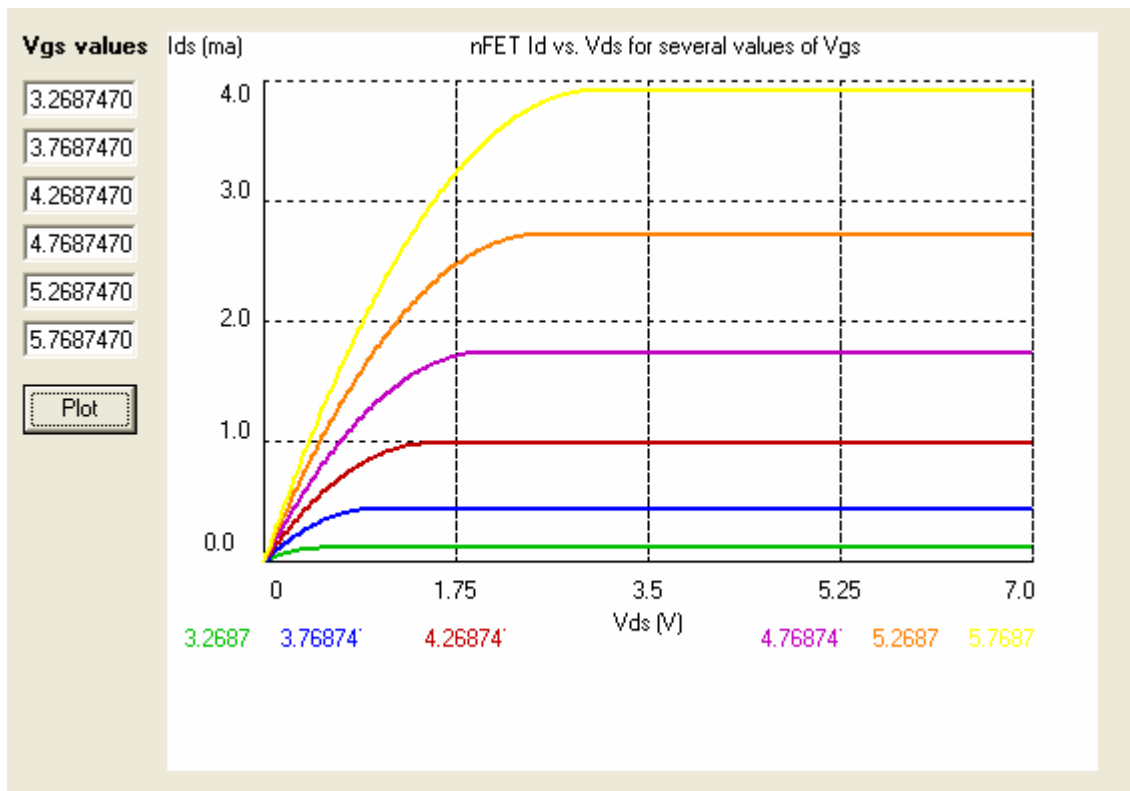


Figure 12. NMOS Characteristic curves

5 Validation

As explained before, the software design tool has been designed to test relative simple inverter structure. Model used for the simulation process is the one considered to behave according to presented equations. Obviously, this simple model will not take in account all possible variables involved in the fabrication process, so DUT performance should be tested at relative higher frequencies.

An alternative inverter design was performed using Microcap Software package. The advantage of using this piece of software was the fact that several basic structure parameters can be change accordingly. The inverter diagram structure is presented in figure 13.

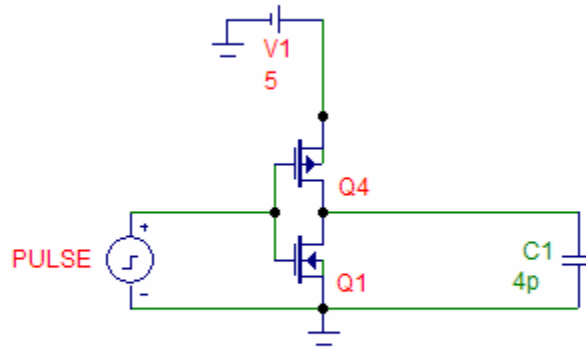


Figure 13. CMOS inverter using Microcap.

This configuration was simulated and tested at three different frequencies (1 MHz, 10 MHz and 100 MHz) and PMOS and CMOS parameters were matched according to the ones used by our Design tool. For relative low frequencies ($f = 1$ MHz) the behavior of

both packages were very closed as expected. Figures 14, 15 depicts output signal for Microcap and our design tool correpondingly.

As expected, Both simulation presents the typical inverter output signal with negligible delays. Even when our design tool was stressed for multiple output sceneario, the output presented no significant delay for up to 20 gates fanout. By the same token, the power consumption was relative small.

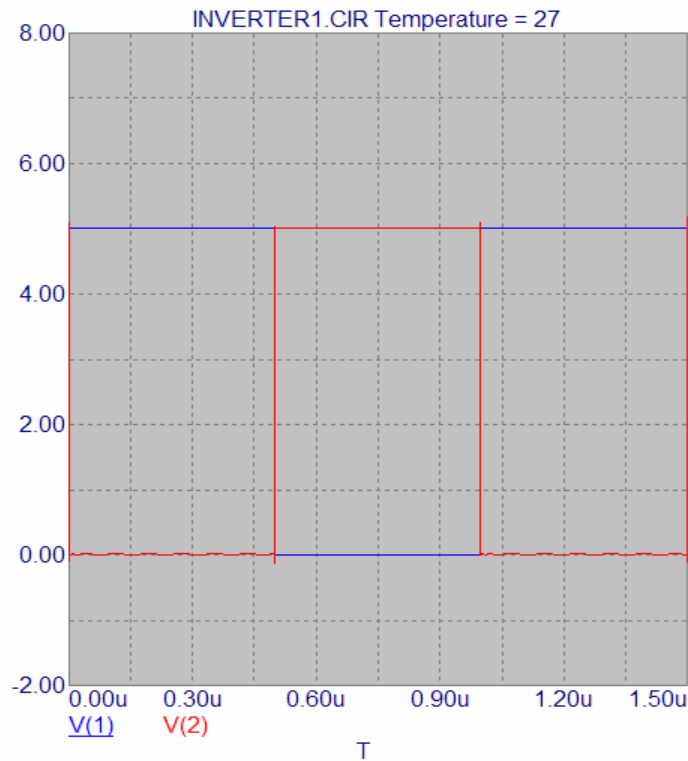


Figure 14. Input/output at f=1 MHz using Microcap

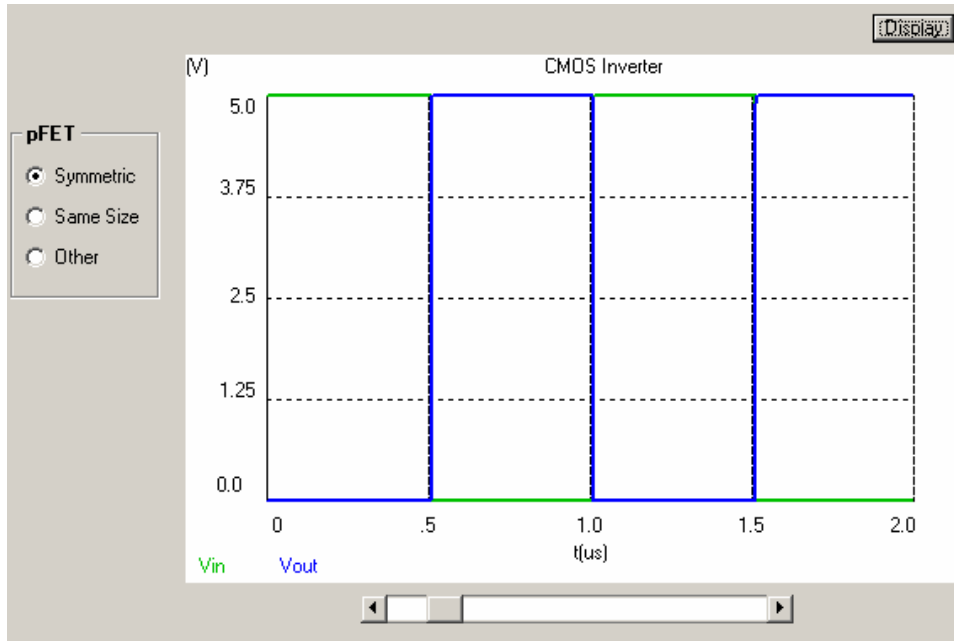


Figure 15. Input/output at $f=1$ MHz using Design tool

The next step on frequency was 10 MHz. This scenario shows very good agreement between the two software tool simulations. Delays are preset for both of them but they remain negligible. Our design tool showed a tighter compromise regarding the fanout capability. Obviously, the power consumed is higher because the frequency increment. Figures 16, 17 depicts output signal for Microcap and our design tool correspondingly.

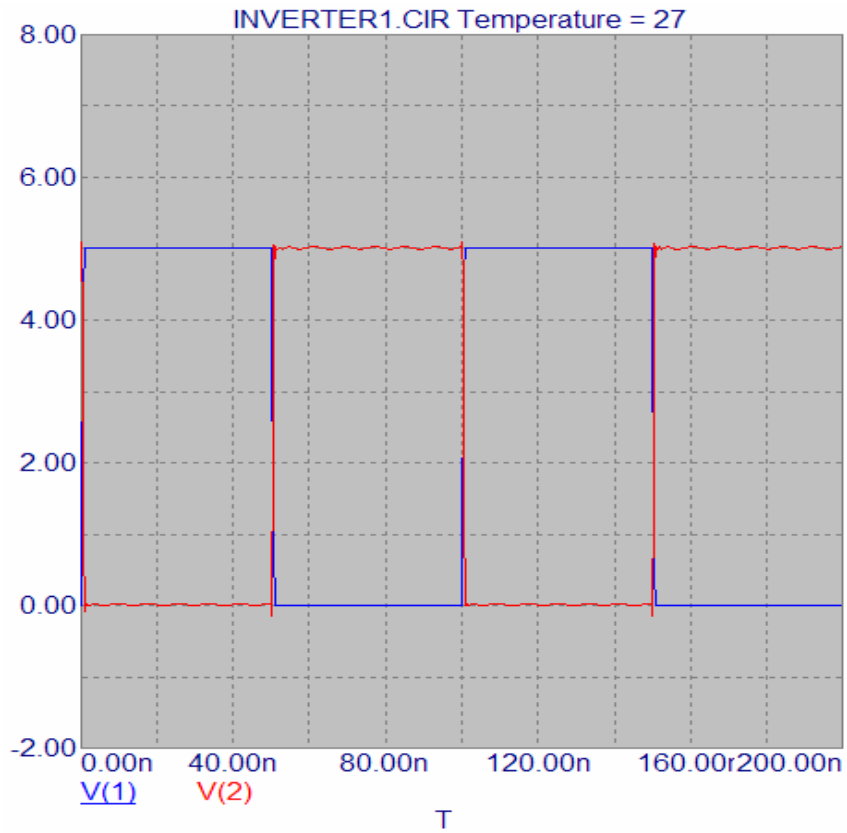


Figure 16. Input/output at $f=10$ MHz using Microcap

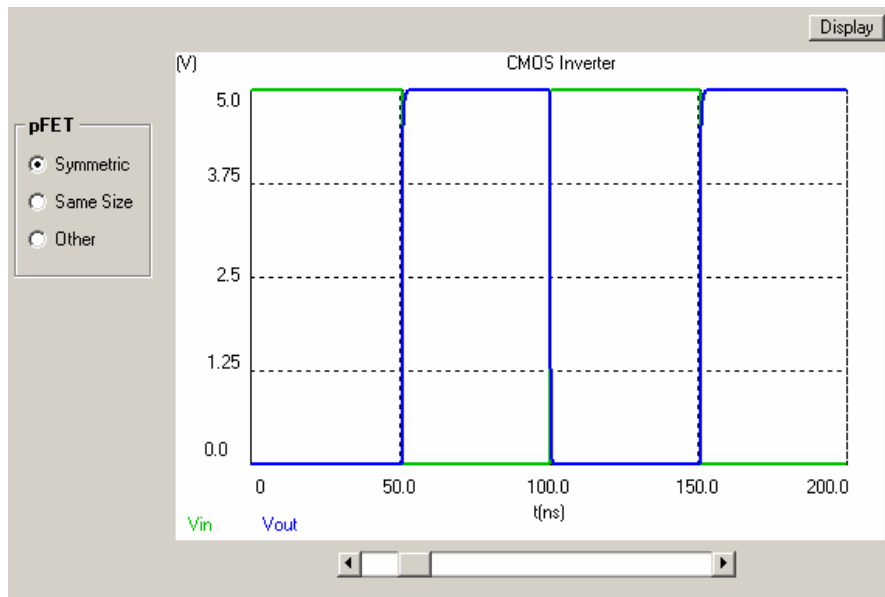


Figure 17. Input/output at $f=10$ MHz using Design tool

The third scenario are plotted in figures 18 and 19.

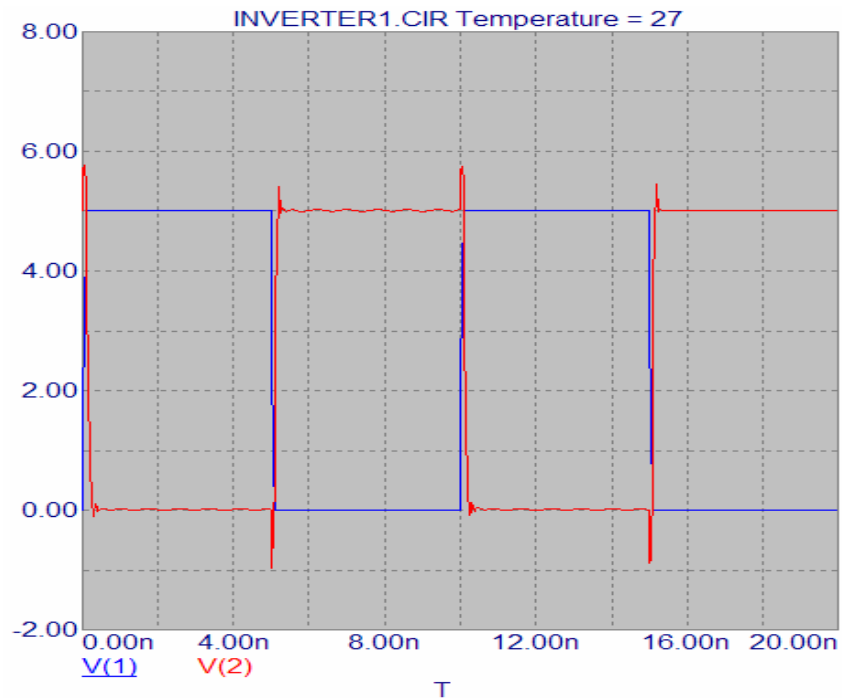


Figure 18. Input/output at $f=100$ MHz using Microcap

This case considered a frequency increment to 100 MHz. the two simulations results present differences and they are based on the high frequency effects that are not completely addressed in our Design tool. Reported Delays are noticeable and for our Design tools, it is not longer negligible. Parasitic effects are not taking in account for our model because the lack of the inductive behavior during the transitions. However, the inverter simulation can still work at this high frequency.

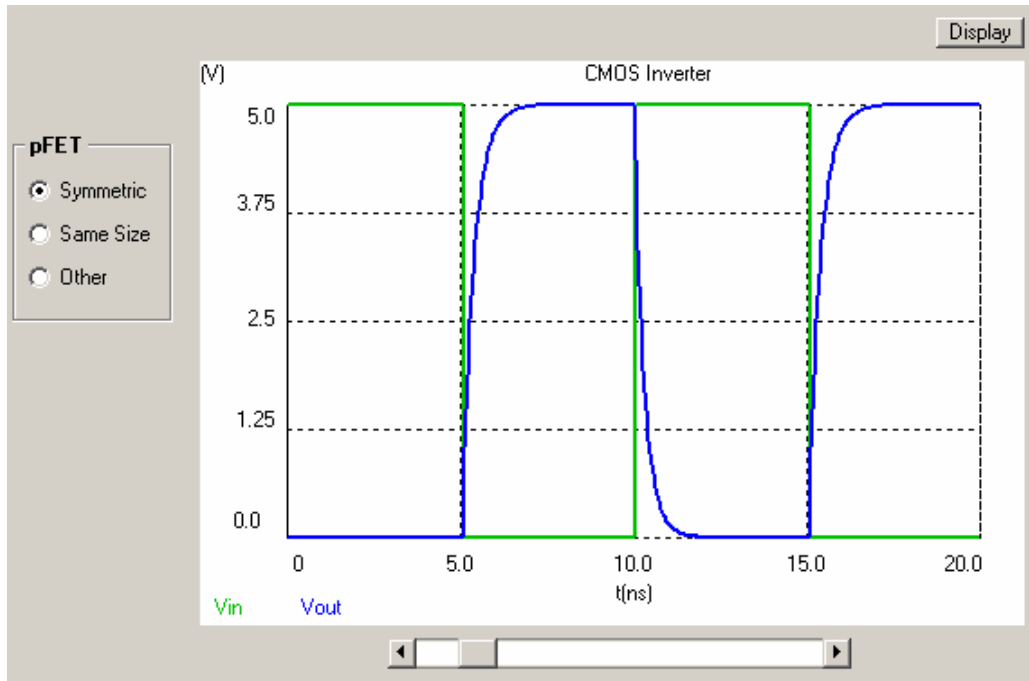


Figure 19. Input/output at $f=100$ MHz using Design tool

6 Conclusions

1. A friendly tool for CMOS design and simulation has been presented. This software application allows the user to understand graphically the basic concepts of the CMOS technology. Proposed model will allow checking for the basic information about the involved physics and fabrication process parameters can be easily interpreted as well.
2. Modeling and simulation are based on physical and electrical behaviors of the analyzed components (MOSFETS). The better understanding of all these

behaviors will lead to a better model representation and closer results after the simulation process. Our Design tools can be improved when corresponding equations can be extended to consider high frequency parameters and interaction among components at large scale integration.

3. Peak consumption occurs at state transition as expected and it is several orders of magnitude higher than the ones at steady state. To built an efficient inverter should take in account the technology used to minimize the currents require to cut or saturate the switch, avoiding to let it be biased in such way that device go deeper on these regions.
4. Designs using discrete devices have poorer performance than Integrated Circuits devices. However, larger densities of transistors will make high power consumption device which maximum fan out should be optimized

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