Problem description:

Understand Clock signals within MSP430

Why need clocks?

- Time elapsed time of events
- Sleep for determined amount of time
- Count events for an amount of time
- Create events to run program

MSP430 Design Workshop

STUDENT GUIDE

Texas Instruments

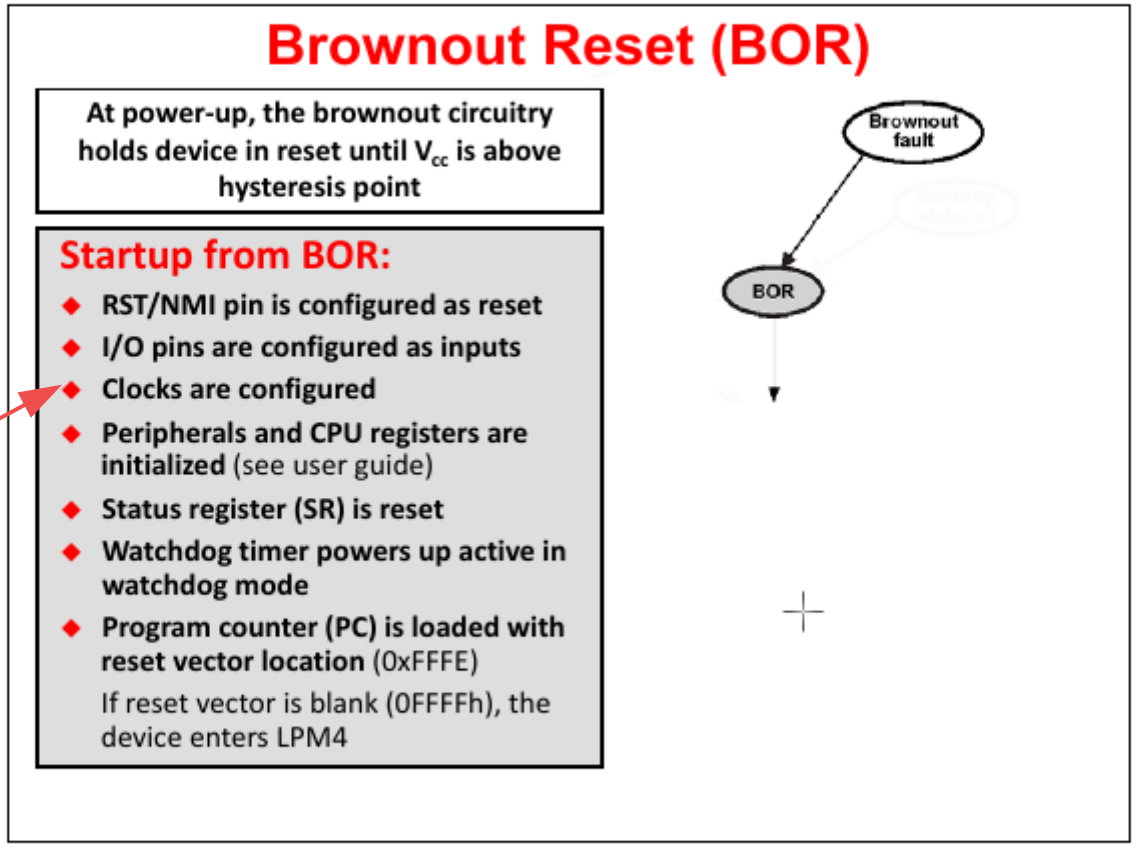
First: What is the default - Power Up Sequence?

Most basic: Power Up Sequence
Most basic of basic – Brown-Out Reset Mode

BOR

The MSP430 starts out in the Brown-Out Reset (BOR) mode. A Brownout Fault (i.e. not enough power) is the most common event that brings the CPU to this state.

All of these are set to default condition



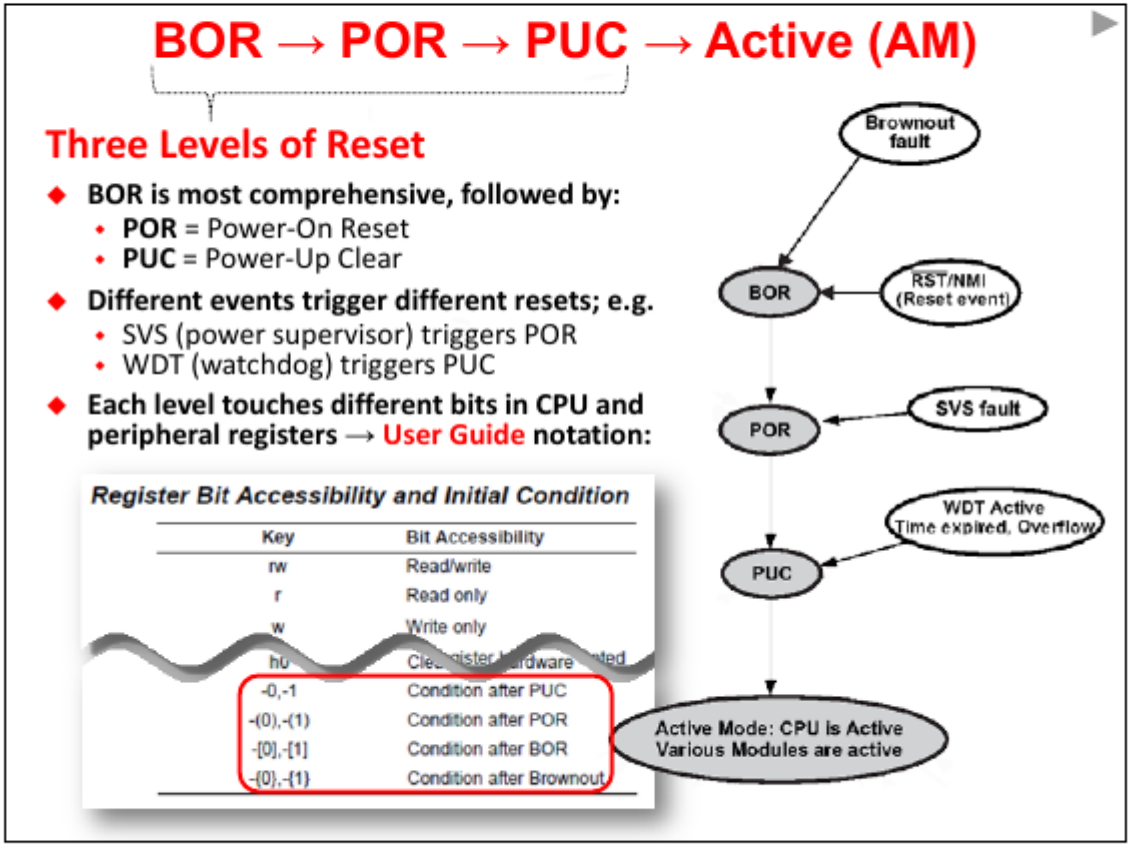
In BOR, a series of items (listed above) are changed to their default states. (As always, the device datasheet and users guide should be the final reference as to what is changed in each of the reset states.)

Power up sequence of events:

Operating Modes (Reset → Active)

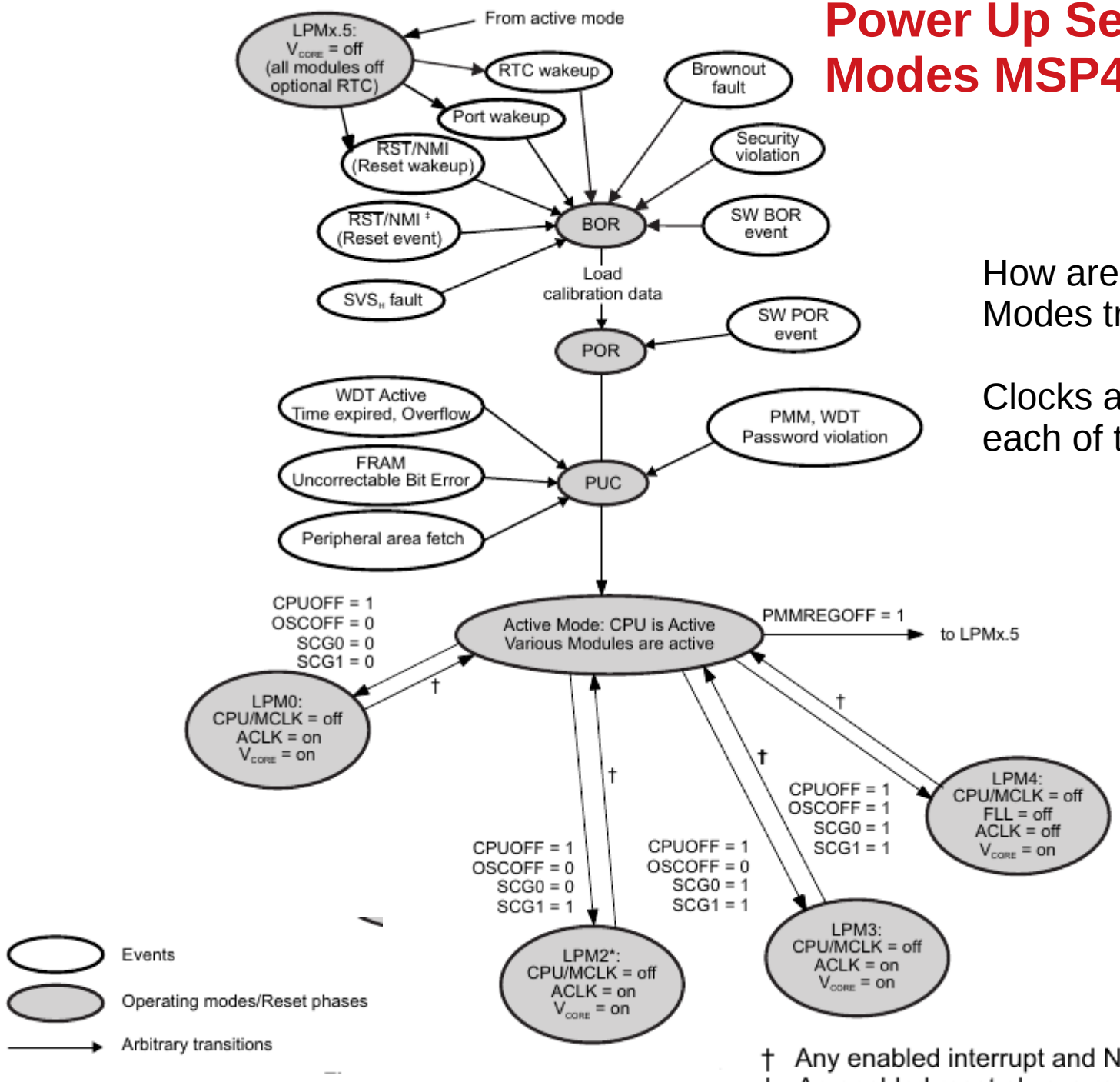
BOR → POR → PUC → Active (AM)

As shown below, BOR is the first of three reset states.



Different reset states, such as BOR, POR and PUC are triggered from different events. For example, upon power-up you may want to do a full system reset; though, this is usually not desired for something like a watchdog timeout event.

Power Up Sequence Modes MSP430FR2433



How are these Power Up Modes triggered?

Clocks are involved in each of these steps

† Any enabled interrupt and NMI performs this transition
‡ An enabled reset always restarts the device

3.3.5 CSCTL4 Register

Clock System Control Register 4

Figure 3-11. CSCTL4 Register

15	14	13	12	11	10	9	8
Reserved							SELA
r0	r0	r0	r0	r0	r0	r0	rw-1
7	6	5	4	3	2	1	0
Reserved					SELMS		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0

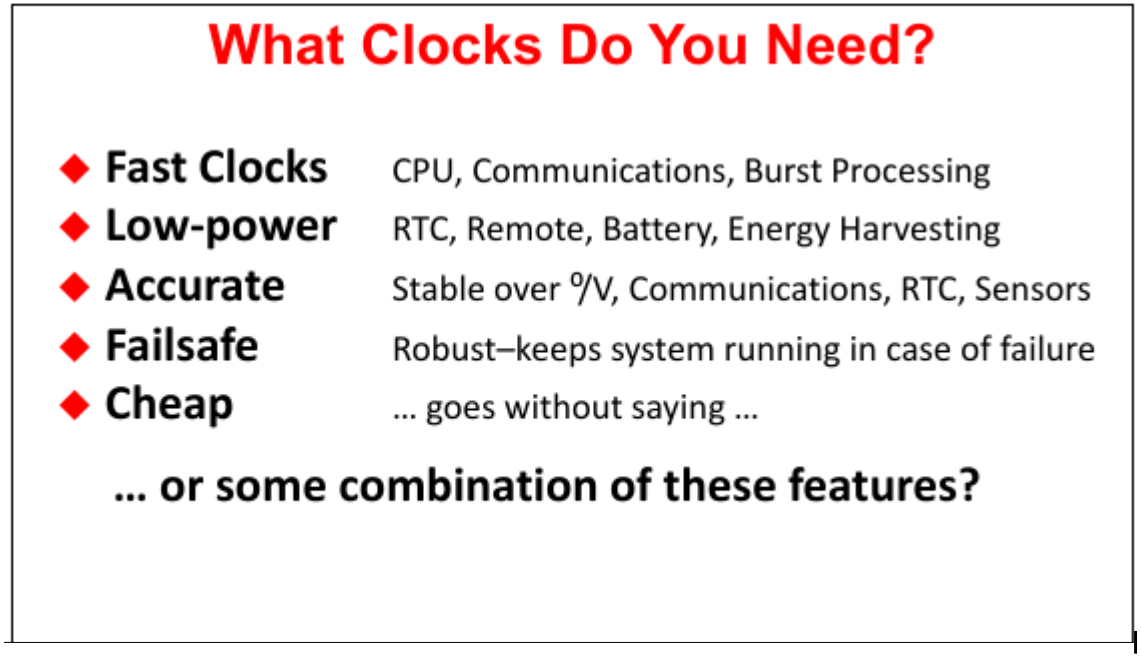
Table 3-7. CSCTL4 Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	SELA	RW	1h	Selects the ACLK source. 0b = XT1CLK with divider (must be no more than 40 kHz) 1b = REFO (internal 32-kHz clock source)
7-3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	SELMS	RW	0h	Selects the MCLK and SMCLK source. 000b = DCOCLKDIV 001b = REFOCLK 010b = XT1CLK 011b = VLOCLK 1xxb = Reserved for future use

Supplying Clock signals for the MSP430FR2433

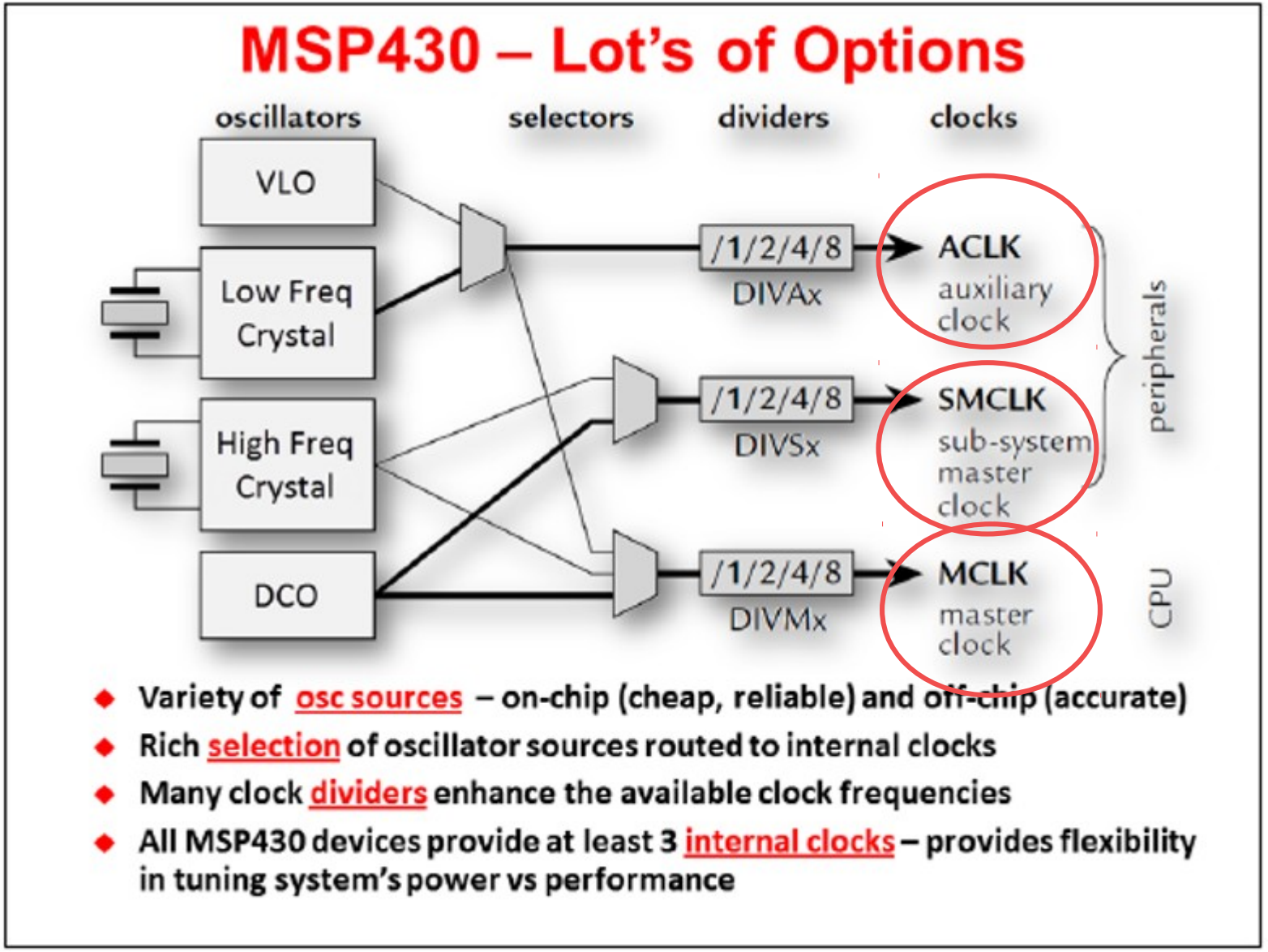
What Clocks Do You Need?

MSP430 provides a wide range of clocking options. Before choosing and configuring the clocks, though, you need to determine which clock features are most important for your system: Fast, low-power, accurate, etc. At times, choosing these various options may force you to make tradeoffs; hence, it's important to for you consider which of these (or what group of them) are most significant for your end-application.



Clock System

Sources **Outputs**



CS Outputs

MCLK, SMCLK, ACLK

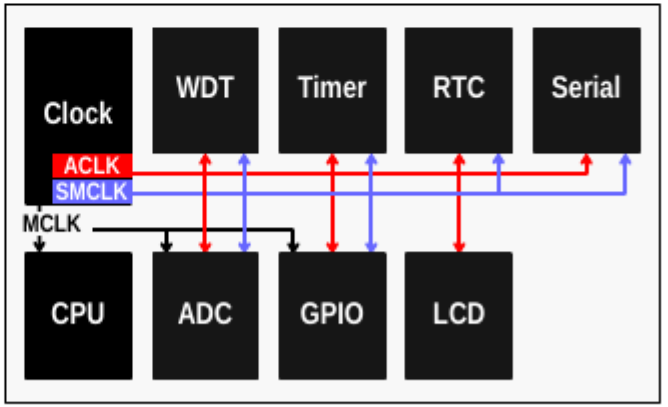
As described in the following graphic, MCLK drives the clock rate of the CPU. It typically runs at a "fast" speed – from 1 MHz up to 16 or 25 MHz (depending upon the upper limit of the given device). MCLK can run slower than this, but it's more common to see the CPU run in the MHz range in order to get its work done quickly and then go into one of the low-power "sleep" modes.

MSP430 Clock Options

Name	Description	Used-by	Typical Speed
❑ **MCLK**	Master Clock	CPU	Fast
❑ **SMCLK**	Sub-Master Clock	Peripherals	Fast
❑ **ACLK**	Auxiliary Clock	Peripherals	Slow

Clocks – Fast or Slow

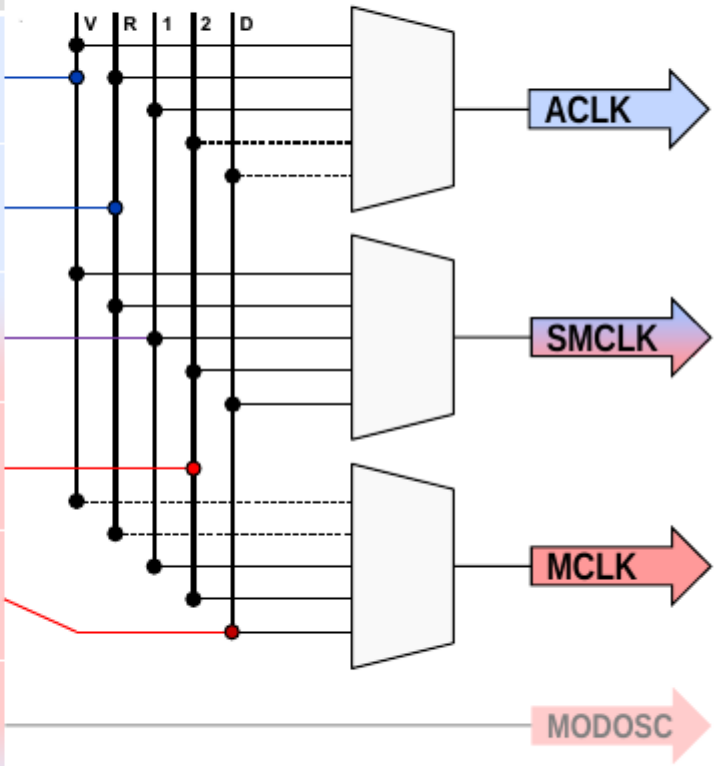
- **All MSP430 devices provide at least 3 clocks**
- **Tune system peripherals by choice of clock:**
  - Fast = Performance
  - Slow = Low-power
- **Fast/slow clocks also provide wider timing**



SMCLK and ACLK are primarily used for clocking peripherals. It's convenient to have two peripheral clocks – one faster (SMCLK) and another slower (ACLK).

MSP430FR2433 Clock Sources

		Frequency
RC	VLO	~10 KHz
	REFO	32768 Hz
32 KHz	XT1	• LF: < 50 KHz • HF: 4-Max MHz
	XT2 not available	
	DCO	100 KHz to CPU Max
Async	MODOSC	• 5 MHz • 5 MHz / 128



*Note: This is a general description, please refer to datasheet/UsersGuide for complete details regarding your device

FR2xx_4xx CS | Clock System

- Four independent clock sources
  - Low Frequency
    - XT1 32768 Hz crystal
    - VLO 10 kHz
  - High Frequency
    - DCO Specific ranges
    - MODCLK Internal 5MHz
- DCO
  - Default = 1MHz
  - FLL with REFO or XT1 reference
- ACLK = Only XT1 or REFO
- SMCLK and MCLK have same source selection
  - Though, SMCLK can be further divided
  - SMCLK can be active even if MCLK is off for LPM
- MODOSC provided to ADC10

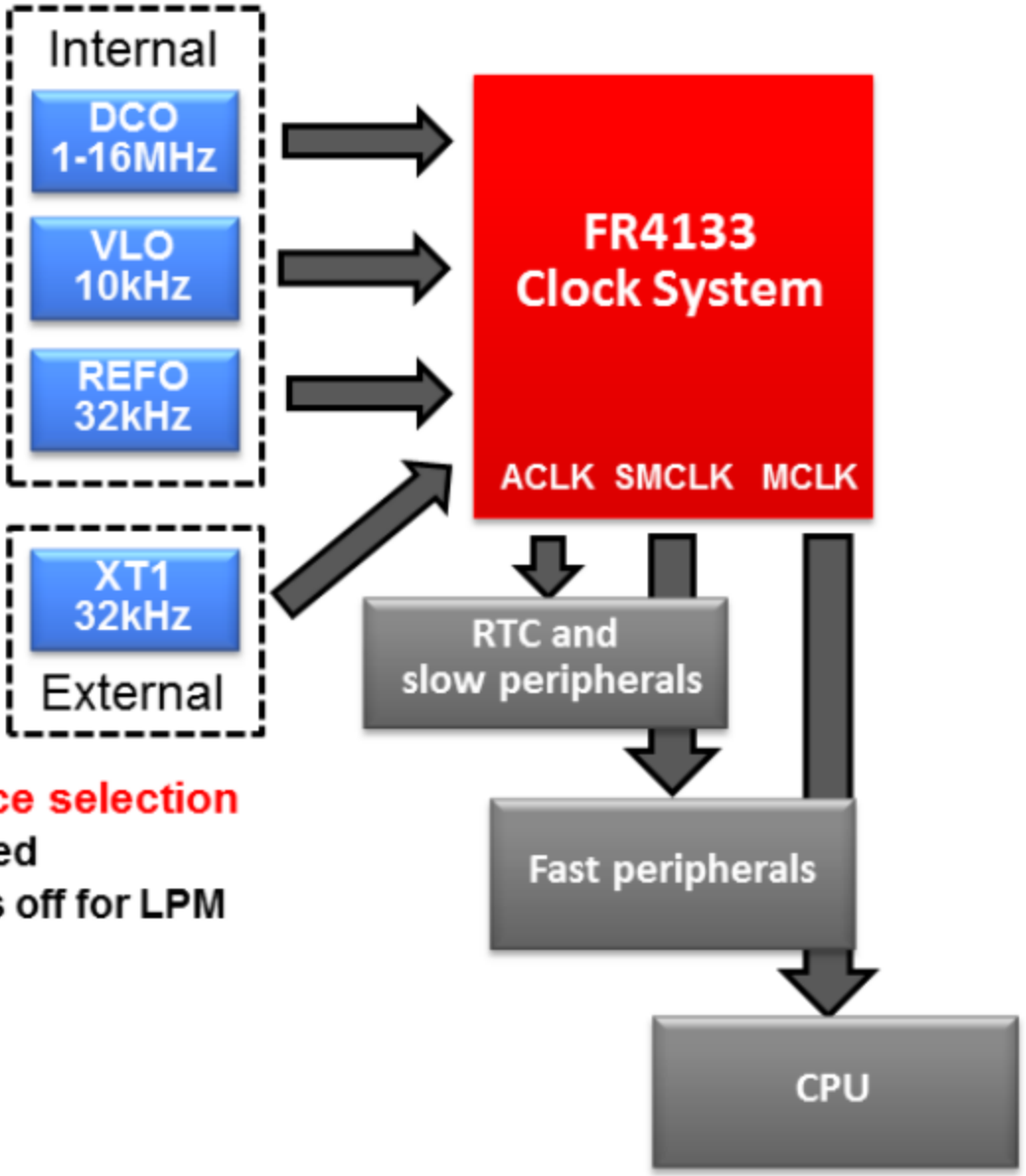


Table 6-7. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	DC to 40 kHz	10 kHz ±50%	

6.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): This clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

Table 6-7. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	DC to 40 kHz	10 kHz ±50%	
CPU	N/A	Default						
FRAM	N/A	Default						
RAM	N/A	Default						
CRC	N/A	Default						
I/O	N/A	Default						
TA0	TASSEL		10b	01b				00b (TA0CLK pin)
TA1	TASSEL		10b	01b				00b (TA1CLK pin)
TA2	TASSEL		10b	01b				
TA3	TASSEL		10b	01b				
eUSCI_A0	UCSSEL		10b or 11b		01b			00b (UCA0CLK pin)
eUSCI_A1	UCSSEL		10b or 11b		01b			00b (UCA1CLK pin)
eUSCI_B0	UCSSEL		10b or 11b		01b			00b (UCB0CLK pin)
WDT	WDTSSEL		00b	01b			10b or 11b	
ADC	ADCSSEL		11b	01b	00b			
RTC	RTCSS		01b			10b	11b	

DCO is Digitally Controlled Oscillator is the High Frequency Source without using a high frequency crystal

FR2xx/4xx DCO Calibration

FR2xx_4xx Clock System (CS)

- DCO setup is hybrid of FR5xx DCO and F5xx DCO + FLL
- Specific frequency ranges
  - Ranges centered on 1, 2, 4, 8, 12, 16MHz
  - Selected with DCORSEL bits
- Uses FLL with reference frequency to tune within frequency range
- 512 DCO steps within these smaller ranges = smaller steps
  - Allows very accurate DCO + FLL even with just REFO – no crystal (+/- 2% over temperature)
  - Even more accurate with crystal (+/-0.5% over temperature)
  - Much less jitter because steps are smaller
- FLL allows compensation for temperature drift

DCO is clock source
Code examples
in following
Timer section

Maximum flexibility for selection of clock sources and speeds

MSP430FR2433 Mixed-Signal Microcontroller

- Clock System (CS)
  - On-Chip 32-kHz RC Oscillator (REFO)
  - On-Chip 16-MHz Digitally Controlled Oscillator (DCO) With Frequency-Locked Loop (FLL)
    - ±1% Accuracy With On-Chip Reference at Room Temperature
  - On-Chip Very Low-Frequency 10-kHz Oscillator (VLO)
  - On-Chip High-Frequency Modulation Oscillator (MODOSC)
  - External 32-kHz Crystal Oscillator (LFXT)
  - Programmable MCLK Prescalar of 1 to 128
  - SMCLK Derived from MCLK With Programmable Prescalar of 1, 2, 4, or 8

Table 3-2. CS Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	CSCTL0	Clock System Control Register 0	Read/write	Word	0000h	Section 3.3.1
02h	CSCTL1	Clock System Control Register 1	Read/write	Word	0033h	Section 3.3.2
04h	CSCTL2	Clock System Control Register 2	Read/write	Word	101Fh	Section 3.3.3
06h	CSCTL3	Clock System Control Register 3	Read/write	Word	0000h	Section 3.3.4
08h	CSCTL4	Clock System Control Register 4	Read/write	Word	0100h	Section 3.3.5
0Ah	CSCTL5	Clock System Control Register 5	Read/write	Word	1000h	Section 3.3.6
0Ch	CSCTL6	Clock System Control Register 6	Read/write	Word	08C1h	Section 3.3.7
0Eh	CSCTL7	Clock System Control Register 7	Read/write	Word	0740h	Section 3.3.8
10h	CSCTL8	Clock System Control Register 8	Read/write	Word	0007h	Section 3.3.9

The Clock System has 9 registers – could represent millions of combinations

We will consider 3 Examples – you can start from these and YMMV
go ahead and modify if needed

Example 1: SMCLK, MCLK = 1 MHz ACLK = 32768 Hz
Power Up Reset settings

Example 2: SMCLK, MCLK = 8 MHz ACLK = 32768 Hz

Example 3: SMCLK, MCLK = 16 MHz ACLK = 32768 Hz

Example 1: MCLK, SMCLK = 1MHz ACLK = 32768Hz

```
1  //******************************************************************************
2  //  MSP430FR243x Demo - Configure MCLK for 8MHz sourced from DCO.
3  //
4  //  Description: Default DCODIV is MCLK and SMCLK source.
5  //  By default on Power Up:
6  //  ACLK = default REFO ~32768Hz, SMCLK = MCLK = f(DCODIV) = 1MHz.
7  //  Toggle LED to indicate that the program is running.
8  //
9  //           MSP430FR2433
10 //         ---------------
11 //     /|\|                 |
12 //      | |                 |
13 //      --|RST              |
14 //        |           P1.0 |---> LED
15 //        |           P1.3 |---> MCLK  = 1MHz
16 //        |           P1.7 |---> SMCLK = 1MHz
17 //        |           P2.2 |---> ACLK  = 32768Hz
18 //
19 //
20 //   Ling Zhu
21 //   Texas Instruments Inc.
22 //   Feb 2015
23 //   Modified by H Watson for Energia  20180702
24 //******************************************************************************
```

Example 1: sketch_msp430fr243x_CS_01MHz.ino

```
26  //   Ling Zhu
27  //   Texas Instruments Inc.
28  //   Feb 2015
29  //   Modified by H Watson for Energia  20180702
30  //******************************************************************************
31  #include <msp430.h>
32
33  int main(void)
34  {
35      WDTCTL = WDTPW | WDTHOLD;               // Stop watchdog timer
36  /* default power on reset condition is SMCLK and MCLK are set at 1.00 MHz
37   *  and the ACLK is 32768Hz
38   *
39   */
40      // details on default values are in SLASE59B datasheet - page 54
41
42      //Use the GPIO pins to output the clock signals - Observe with Oscilloscope
43      P1DIR |= BIT0 | BIT3 | BIT7;             // set LED MCLK and SMCLK pins as outputs
44      P1SEL1 |= BIT3 | BIT7;                   // set MCLK and  SMCLK pins as second function
45                                               //  (P1SEL0 is 0 from POR) so connect them to MCLK, SMCLK
46      P2DIR |= BIT2;                           // set ACLK pin as output
47      P2SEL1 |= BIT2;                          // set ACLK pin as second function
48
49      PM5CTL0 &= ~LOCKLPM5;                    // Disable the GPIO power-on default high-impedance mode
50                                               // to activate previously configured port settings
51
52      while(1)
53      {
54          P1OUT ^= BIT0;                       // Toggle P1.0 using exclusive-OR
55          __delay_cycles(10000000);            // Delay for 10000000*(1/MCLK)=1.25s
56      }
57  }
58
```

Example 2: MCLK, SMCLK = 8MHz ACLK = 32768Hz

```
1  //*****************************************************************************
2  //  MSP430FR243x Demo - Configure MCLK for 8MHz sourced from DCO.
3  //
4  //  Description: Default DCODIV is MCLK and SMCLK source.
5  //  By default, FR243x select XT1 as FLL reference.
6  //  If XT1 is present, the XIN and XOUT pin needs to configure.
7  //  If XT1 is absent, switch to select REFO as FLL reference automatically.
8  //  XT1 is considered to be absent in this example.
9  //  f(DCOCLK) = 2^FLLD * (FLLN+1) * (fFLLREFCLK / n).
10 //  FLLD = 0, FLLN =243, n=1, DIVM =1, f(DCOCLK) = 2^0 * (243+1)*32768Hz = 8MHz,
11 //  f(DCODIV) = (243+1)*32768Hz = 8MHz,
12 //  ACLK = default REFO ~32768Hz, SMCLK = MCLK = f(DCODIV) = 8MHz.
13 //  Toggle LED to indicate that the program is running.
14 //
15 //           MSP430FR2433
16 //         ---------------
17 //     /|\|               |
18 //      | |               |
19 //      --|RST            |
20 //        |          P1.0 |---> LED
21 //        |          P1.3 |---> MCLK  = 8MHz
22 //        |          P1.7 |---> SMCLK = 8MHz
23 //        |          P2.2 |---> ACLK  = 32768Hz
24 //
25 //
26 //   Ling Zhu
27 //   Texas Instruments Inc.
28 //   Feb 2015
29 //   Modified by H Watson for Energia 20180702
30 //*****************************************************************************
```

Example 2: sketch_msp430fr243x_CS_08MHz.ino

```
31  #include <msp430.h>
32
33  int main(void)
34  {
35      WDTCTL = WDTPW | WDTHOLD;                 // Stop watchdog timer
36
37      // set MCLK, SMCLK to 8 MHz using DCO as source
38      __bis_SR_register(SCG0);                  // disable FLL
39      CSCTL3 |= SELREF__REFOCLK;                // Set REFO as FLL reference source
40      CSCTL0 = 0;                               // clear DCO and MOD registers
41      CSCTL1 &= ~(DCORSEL_7);                   // Clear DCO frequency select bits first
42      CSCTL1 |= DCORSEL_3;                      // Set DCO = 8MHz
43      CSCTL2 = FLLD_0 + 243;                    // DCODIV = 8MHz
44      __delay_cycles(3);
45      __bic_SR_register(SCG0);                  // enable FLL
46      while(CSCTL7 & (FLLUNLOCK0 | FLLUNLOCK1)); // Poll until FLL is locked
47
48
49      CSCTL4 = SELMS__DCOCLKDIV | SELA__REFOCLK; // set default REFO(~32768Hz) as ACLK source, ACLK = 32768Hz
50                                                // default DCODIV as MCLK and SMCLK source
51      // details on these values are in SLASE59B datasheet - page 54
52      P1DIR |= BIT0 | BIT3 | BIT7;              // set MCLK SMCLK and LED pin as output  125nsec
53      P1SEL1 |= BIT3 | BIT7;                    // set MCLK and  SMCLK pin as second function (P1SEL0=0 from POR)
54      P2DIR |= BIT2;                            // set ACLK pin as output
55      P2SEL1 |= BIT2;                           // set ACLK pin as second function
56
57      PM5CTL0 &= ~LOCKLPM5;                     // Disable the GPIO power-on default high-impedance mode
58                                                // to activate previously configured port settings
59
60      while(1)
61      {
62          P1OUT ^= BIT0;                        // Toggle P1.0 using exclusive-OR
63          __delay_cycles(10000000);             // Delay for 10000000*(1/MCLK)=1.25s
64      }
65  }
66
```

Example 3: MCLK, SMCLK = 16MHz ACLK = 32768Hz

```
1  //******************************************************************************
2  //  MSP430FR243x Demo - Configure MCLK for 16MHz operation, and REFO sourcing
3  //                                      FLLREF and ACLK.
4  //
5  //  Description: Configure MCLK for 16MHz. FLL reference clock is REFO. At this
6  //                    speed, the FRAM requires wait states.
7  //                    ACLK = default REFO ~32768Hz, SMCLK = MCLK = 16MHz.
8  //                    Toggle LED to indicate that the program is running.
9  //
10 //           MSP430FR2433
11 //         ---------------
12 //     /|\|                |
13 //      | |                |
14 //      --|RST             |
15 //        |          P1.0 |---> LED
16 //        |          P1.3 |---> MCLK  = 16MHz
17 //        |          P1.7 |---> SMCLK = 16MHz
18 //        |          P2.2 |---> ACLK  = 32768Hz
19 //
20 //
21 //   Ling Zhu
22 //   Texas Instruments Inc.
23 //   Feb 2015
24 //   Modified by H Watson for Energia  20180702
25 //******************************************************************************
```

Example 3: sketch_msp430fr243x_CS_16MHz.ino

```
26  #include <msp430.h>
27
28  int main(void)
29  {
30      WDTCTL = WDTPW | WDTHOLD;                       // Stop watchdog timer
31
32      // Configure one FRAM waitstate as required by the device datasheet for MCLK
33      // operation beyond 8MHz _before_ configuring the clock system.
34      FRCTL0 = FRCTLPW | NWAITS_1;
35
36      __bis_SR_register(SCG0);                        // disable FLL
37      CSCTL3 |= SELREF__REFOCLK;                      // Set REFO as FLL reference source
38      CSCTL0 = 0;                                     // clear DCO and MOD registers
39      CSCTL1 &= ~(DCORSEL_7);                         // Clear DCO frequency select bits first
40      CSCTL1 |= DCORSEL_5;                            // Set DCO = 16MHz
41      CSCTL2 = FLLD_0 + 487;                          // DCOCLKDIV = 16MHz
42      __delay_cycles(3);
43      __bic_SR_register(SCG0);                        // enable FLL
44      while(CSCTL7 & (FLLUNLOCK0 | FLLUNLOCK1));      // FLL locked
45
46      CSCTL4 = SELMS__DCOCLKDIV | SELA__REFOCLK;      // set default REFO(~32768Hz) as ACLK source, ACLK = 32768Hz
47                                                      // default DCOCLKDIV as MCLK and SMCLK source
48
49      P1DIR |= BIT0 | BIT3 | BIT7;            // set MCLK SMCLK and LED pin as output
50      P1SEL1 |= BIT3 | BIT7;                  // set MCLK and  SMCLK pin as second function
51      P2DIR |= BIT2;                          // set ACLK pin as output
52      P2SEL1 |= BIT2;                         // set ACLK pin as second function
53
54      PM5CTL0 &= ~LOCKLPM5;                           // Disable the GPIO power-on default high-impedance mode
55                                                      // to activate previously configured port settings
56
57      while(1)
58      {
59          P1OUT ^= BIT0;                              // Toggle P1.0 using exclusive-OR
60          __delay_cycles(8000000);                    // Delay for 8000000*(1/MCLK)=0.5s
61      }
62  }
```