Leakage Temperature Dependency Modeling in System Level Analysis

Huang Huang, Gang Quan, Jeffrey Fan
Florida International University
10555 W Flagler Street, Miami, FL 33174, USA

Abstract— As the semiconductor technology continues its marching toward the deep sub-micron domain, the strong relation between leakage current and temperature becomes critical in power-aware and thermal-aware design for electronic systems. Previous circuit-level research results can capture the leakage/temperature dependency accurately, but can be too complex and thus ineffective in high level system design. In this paper, we study a large spectrum of leakage power models that are able to account for the leakage/temperature dependency, and in the meantime, are simple enough and suitable for system level design. We analyze and compare the tradeoff between the complexity and accuracy of these models empirically. Our experimental results strengthen the important role that the leakage power consumption plays in the electronic system design as the transistor size continues to shrink. More importantly, our results highlight the fact that it is vital to take the leakage/temperature and leakage/supply voltage dependency into considerations for high level power and thermal aware system level design.

Keywords— Leakage power, leakage/temperature dependency, power aware, thermal aware, system level design

I. Introduction

The power consumption of the processors has been growing exponentially with each technology generation, expecting to grow continuously and rapidly in the future [1]. The soaring power consumption of processors has posed challenges, not only on how to provide enough power source for a system, but also on how to manage the heat generated by the system. Power-aware designs have been researched extensively in the past decade [2], crossing different abstraction levels and platforms. However, power-aware design techniques alone cannot address all thermal issues [3–5]. The escalating heat in such systems may incur high packaging and cooling costs, and threaten to degrade the performance, life span, and reliability of computing systems significantly [6, 7]. Therefore, as processors power consumption continues to rise, thermal management has also become a critical issue in the design of high-quality computing systems.

As semiconductor technology continues to scale down, the leakage plays a increasingly important role [8, 9]. This is particularly true since the leakage power is comparable or even dominates the dynamic power consumption in the deep sub-micron circuits [8, 10]. In addition, there is a strong relationship between leakage and temperature. The higher the temperature, the larger the leakage current becomes. Liao et al. [8] shows that the leakage power can increase as much as 38% when temperature changes from 65^oC to 110^oC. As the leakage power becomes more prominent, the increase of leakage will in turn increase the overall power consumption significantly. The increased power consumption will elevate the temperature to an even higher level and increase the leakage power consumption. Therefore, this temperature/leakage feedback loop must be properly addressed when developing the power-aware and thermal-aware techniques to ensure that they can really be effective in quality electronic system design.

The circuit-level analysis [8, 9] indicates that the leakage power varies with temperature and supply voltage in a very complex manner. According to [8], the leakage current I_{leak} can be formulated as

$$I_{leak} = I_s \cdot (\mathcal{A} \cdot T^2 \cdot e^{((\alpha \cdot V_{dd} + \beta)/T)} + \mathcal{B} \cdot e^{(\gamma \cdot V_{dd} + \delta)}) \quad (1)$$

where I_s is the leakage current at certain reference temperature and supply voltage. T is the operating temperature and V_{dd} is the operating supply voltage. $\mathcal{A}$, $\mathcal{B}$, α, β, γ and δ are empirically determined technology constants. Some thermal analysis tools developed based on this model, such as the "HotSpot" [11], can be effectively used to simulate and study the thermal phenomena at the circuit and architecture level.

Due to its non-linear and high-order-magnitude terms, using equation 1 directly for high level analysis can be very challenging. While some researches [4,12–14] have adopted equation (1) for high-level analysis, the complexity of this model has significantly limited the depth and scope of its applicability in system level design. For example, some formulated the thermal management problem as a non-linear optimization problem [4, 13] by incorporating equation (1) in formulating the constraints. The problem is that the computational complexity of the non-linear optimization becomes very high. Therefore these approaches can only work at the system level when the design space is small.

On the other hand, Liu et al. [15] showed that the leakage current changes with temperature super linearly [15]. This presents a great opportunity to simplify the leakage model in system level analysis. Based on this observation, a few leakage/temperature dependency models have been proposed [16, 17], which greatly simplify the leakage power computation and are suitable for system level thermal analysis.

In system level analysis, an important decision that has to be made is the tradeoff between the complexity and ac-

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curacy of a model. This is particularly true for choosing appropriate leakage models for system-level thermal analysis, where temperature changes non-linearly with power consumption. A linear but complicated leakage/temperature model can still make the thermal problem untractable even though it has simplified the leakage/temperature relationship tremendously. On the other hand, the analysis results and techniques developed based on a model can deviate farther away from reality if the leakage/temperature model is not accurate enough. Therefore, there is a compelling reason to study the accuracy and complexity tradeoff for different leakage/temperature models.

In this paper, we propose to examine six different leakage models that use linear functions to capture the leakage/temperature characteristics. Based on technical parameters for 65nm IC technology published in the literature [8], we study the accuracy of the models and their potential impacts on the thermal analysis. Our experimental results show that there exist dramatically large difference in terms of estimation and accuracy among different leakage models. In addition, such differences can turn into significant discrepancies in system level thermal analysis. Therefore, choosing appropriate leakage models is vital in power related and thermal-aware system level analysis.

The rest of the paper is organized as follows. In Section 2, we introduce the technical background related to our research. We discuss different leakage models in Section 3. In Section 4, we discuss our experimental results. We draw the conclusions in Section 5.

II. Preliminary

We consider a processor with k different running modes. Each mode $i(1 \leq i \leq k)$ is characterized by a supply voltage v_i and its corresponding working frequency f_i. For system level thermals analysis, we adopted the widely used RC thermal model to capture the temperature dynamics for a processor (e.g. [12, 16–18]):

$$RC\frac{dT(t)}{dt} + T(t) - RP(t) = T_{amb}, \tag{2}$$

where T_{amb} is the ambient temperature, $P(t)$ denotes the power consumption (in $Watt$) at time t, and R, C denote the thermal resistance (in $J/^oC$) and thermal capacitance (in $Watt/^oC$). By scaling T such that T_{amb} is zero, we have

$$\frac{dT(t)}{dt} = aP(t) - bT(t), \tag{3}$$

where $a = 1/C$ and $b = 1/RC$. From equation (3), we can see that temperature varies with temperature in an exponential manner.

Assuming that all processor running modes are safe and do not cause processor temperature to "run away", i.e. the scenarios when the processor temperature increases indefinitely, the temperature becomes gradually stable if the processor runs in one mode long enough. Consider the processor stable status, we have

$$\frac{dT(t)}{dt} \to 0. \tag{4}$$

As a result, from equation (3), when the processor temperature becomes stable at T_{max}, we have

$$aP(v) - bT_{max}(v) \to 0, \tag{5}$$

or

$$\triangle T_{max}(v) = \frac{a}{b} \triangle P(v). \tag{6}$$

Equation (6) shows the relationship between the estimation error of the stable temperature and overall power consumption. As an example, for the conventional air cooling option, we have $Rth = 0.8K/W$ and $Cth = 340J/K$ [6], and thus we have

$$\triangle T_{max}(v) = 0.8 \triangle P(v). \tag{7}$$

From equation (7), to ensure an accurate thermal analysis result, we need to model the processor power consumption accurately.

The processor power consumption is composed of two parts, i.e. dynamic P_{dyn} and leakage P_{leak},

$$P = P_{dyn} + P_{leak}. \tag{8}$$

The dynamic power consumption, P_{dyn}, is independent to temperature variations, and can be formulated as $P_{dyn} \propto v_{dd}^{\xi}(k)(\xi > 1)$. The leakage power consumption, on the other hand, depends on temperature and can be formulated as:

$$P_{leak} = N_{gate} \cdot I_{leak} \cdot v_{dd} \tag{9}$$

where N_{gate} represents the number of gates, v_{dd} is the voltage level, and I_{leak} is the leakage current. I_{leak} varies with both temperature and supply voltage and can be calculated with equation (1). While using equation (1) can accurately estimate the leakage current, with relative error less than 1% [8], it is too complicated to be used for high level system analysis due to its high order and exponential terms. Liu et al. [15] found that using linear approximation can estimate the leakage with a reasonable accuracy, i.e. with error within 1% using the piece-wise linear function or less than 5.5% using single linear function.

In what follows, we derive six different linear leakage models, and study their complexity/accuracy tradeoffs in power and thermal-aware system level analysis.

III. Linear leakage/tempearture models

Since leakage power consumption depends on both temperature and supply voltage, a general polynomial model to simplify the leakage/temperature dependency can be formulated as

$$P_{leak} = c_0 + c_1 T + c_2 v_{dd} + c_3 T v_{dd}, \tag{10}$$

where c_0, c_1, c_2, c_3 are constants. In this section, we develop six leakage models, Model 1 to Model 6, based on equation (10), to simplify the leakage/temperature relationship.

- **Model 1** can be formulated as follows:

$$P_{leak}(i) = C_0, \tag{11}$$

TABLE I
LEAKAGE MODEL DEFINITION

Model #	Formula	Description
Model 0	$P_{leak} = V_{dd} \cdot (I_s \cdot (\mathcal{A} \cdot T^2 \cdot e^{((\alpha \cdot V_{dd} + \beta)/T)} + \mathcal{B} \cdot e^{(\gamma \cdot V_{dd} + \delta)}))$	Non-linear leakage model
Model 1	$P_{leak}(i) = C_0$	Constant leakage model
Model 2	$P_{leak}(i) = C_0 + C_1 T$	Leakage depends on temperature only
Model 3	$P_{leak}(i) = C_0(i) + C_1(i) v_i$	Leakage depends on supply voltage only
Model 4	$P_{leak}(i) = C_0(i) + C_1(i) v_i + C_2 T$	Leakage depends on both supply voltage and temperature, but leakage increases with temperature uniformly.
Model 5	$P_{leak}(i) = C_0 + (C_1(i) + C_2(i) T) v_i$	Leakage varies with supply voltage and temperature non-uniformly.
Model 6	$P_{leak}(i) = \begin{cases} C_{00} + (C_{10}(i) + C_{20}(i) T) v_i, & T \le T_z \\ C_{01} + (C_{11}(i) + C_{21}(i) T) v_i & T > T_z \end{cases}$	Two-segment piecewise linear model. Each segment is obtained by the same method with Model 5

where $P_{leak}(i)$ denotes the leakage power consumption with running processor in mode i. In this model, the leakage power is assumed to be a constant, and depends on neither temperature nor supply voltage. This is the simplest leakage model.

- **Model 2** can be formulated in equation (12).

$$P_{leak}(i) = C_0 + C_1 T \tag{12}$$

This model assumes that the leakage power varies with temperature linearly but not with supply voltage. This model is adopted in a number of recent researches (e.g. [16]).

- **Model 3** is formulated in equation (13).

$$P_{leak}(i) = C_0(i) + C_1(i) v_i. \tag{13}$$

In contrast to Model 2, this model assumes that the leakage power changes linearly with supply voltage but not with temperature.

- **Model 4** is formulated in equation (14).

$$P_{leak}(i) = C_0(i) + C_1(i) v_i + C_2 T \tag{14}$$

This model improves upon Model 2 and Model 3 by assuming that the leakage power varies not only with supply voltage but also with temperature. Note that, C_2 in equation (14) is a constant independent of i. Therefore the leakage power consumption estimated based on equation (14) increases uniformly at the same rate with respect to temperature.

- **Model 5** also assumes the leakage power consumption varies with both temperature and supply voltage, as formulated in equation (15).

$$P_{leak}(i) = C_0 + (C_1(i) + C_2(i) T) v_i \tag{15}$$

This model is first proposed in [17]. The difference between Model 4 and Model 5 is that Model 5 assumes the leakage power varies at different rates with temperature based on different supply voltages, while Model 4 assumes a uniform rate.

- **Model 6** uses a piece-wise linear function rather than a single linear function to approximate the leakage/temperature relationship, as formulated in equation (16).

$$P_{leak}(i) = \begin{cases} C_{00} + (C_{10}(i) + C_{20}(i) T) v_i, & T \le T_z \\ C_{01} + (C_{11}(i) + C_{21}(i) T) v_i & T > T_z \end{cases} \tag{16}$$

Specifically, equation (16) adopted a piecewise linear function consisting of two linear functions, with T_z as the conjunction point. When the temperature is lower than T_z, the first linear function is used to estimate the leakage power consumption, or the second one otherwise.

For the sake of comparison, we call the leakage model that is based on equation (1) as Model 0. Table I summarizes all seven leakage models. It is not difficult to see from Table I that, while different leakage models (i.e. Model 1 to Model 6) have different complexities, they all have greatly simplified the complex leakage/temperature relationship as described in Model 0 and hence more suitable for system level analysis.

The question now becomes how accurate these models are when used for leakage power estimation at the system level, and how effective they can be in system level design of power and thermal management techniques. It is difficult to compare the accuracy of these models since the constants in Table I are obtained through curve-fitting methods rather than from certain analytical formulas. In the next section, we launched a series of experiments to answer these questions.

IV. Experimental results

We conducted two sets of experiments to validate the leakage models introduced above. In the first set of experiments, we compared the leakage power consumptions at different temperatures and different supply voltages using different models, i.e. Model 1 to Model 6. Using Model

0 as the base line results, we compared the average and maximal estimation errors by different linear leakage models. This set of experiments help to identify the accuracy of each linear leakage model.

To study how a proposed leakage model may impact on the system level power and thermal analysis, we launched the second set of experiments, in which we compared the peak temperature estimated by different leakage models for a processor running with single processor speed.

A. Experiment setup

In our experiments, we built our processor model based on the technical parameters drawn from the 65nm IC technology [8]. We assume that the supply voltage can change from 0.6 Volt to 1.3 Volt with step size of 0.05 Volt, and thus the processor can work in total $k = 15$ modes. The number of gates, i.e. N_{Gate} in Equation (9), is set to be 1×10^6. We set the temperature from 40 ^oC to 110 ^oC with step size of 5^oC. For the thermal constants, we selected $R_{th} = 0.8K/W$, $C_{th} = 340J/K$, and the ambient temperature was set to 25^oC. The dynamic power consumption was determined based on experimental results reported in [8] on a common benchmark *gcc*.

The six leakage power models discussed in Section 3 were constructed. The constants in each models were determined based on the leakage power consumptions at different temperatures and supply voltages calculated with Model 0. In Model 1, constant C_0 is determined to be the leakage power at the ambient temperature. To obtain the constants C_0 and C_1 in Model 2, we first used linear approximation for leakage power consumption at each supply voltage v_i and obtained a pair of parameters of $C_0(i)$ and $C_1(i)$. We then took the average value as the C_0 and C_1. The constants in Model 3, 4, 5 were determined by linear approximation methods based on the leakage power consumption at different supply voltages. In Model 7, we picked the middle point, $Tz = 75^oC$, as the conjunction temperature. We then used curve-fitting to determine the corresponding constants in equation (16).

B. Leakage power estimation

In our first set of experiments, we collected the estimated leakage power consumptions by each model at different supply voltages and temperatures. We used these results to compare with those by Model 0, as plotted in Figure 1. In the meantime, we also collected the absolute estimation error (AEE) and relative estimation error (REE) for each model, with the average and maximal values summarized in Table II. Specifically, the absolute error (i.e. $AEE(M_i)$) and relative error (i.e. $REE(M_i)$) are defined as follows:

$$AEE(M_i) = |P_{leak}[M_i] - P_{leak}[M_0]| \quad (17)$$

$$REE(M_i) = \frac{AEE(M_i)}{P_{leak}[M_0]} \quad (18)$$

where $P_{leak}[M_i]$ is the leakage power estimation based on Model i. The average and maximal values in Table II are obtained among all k different running modes. That is,

$$AEE(Avg) = \frac{\sum_{i=1}^{k} AEE(M_i)}{k} \quad (19)$$

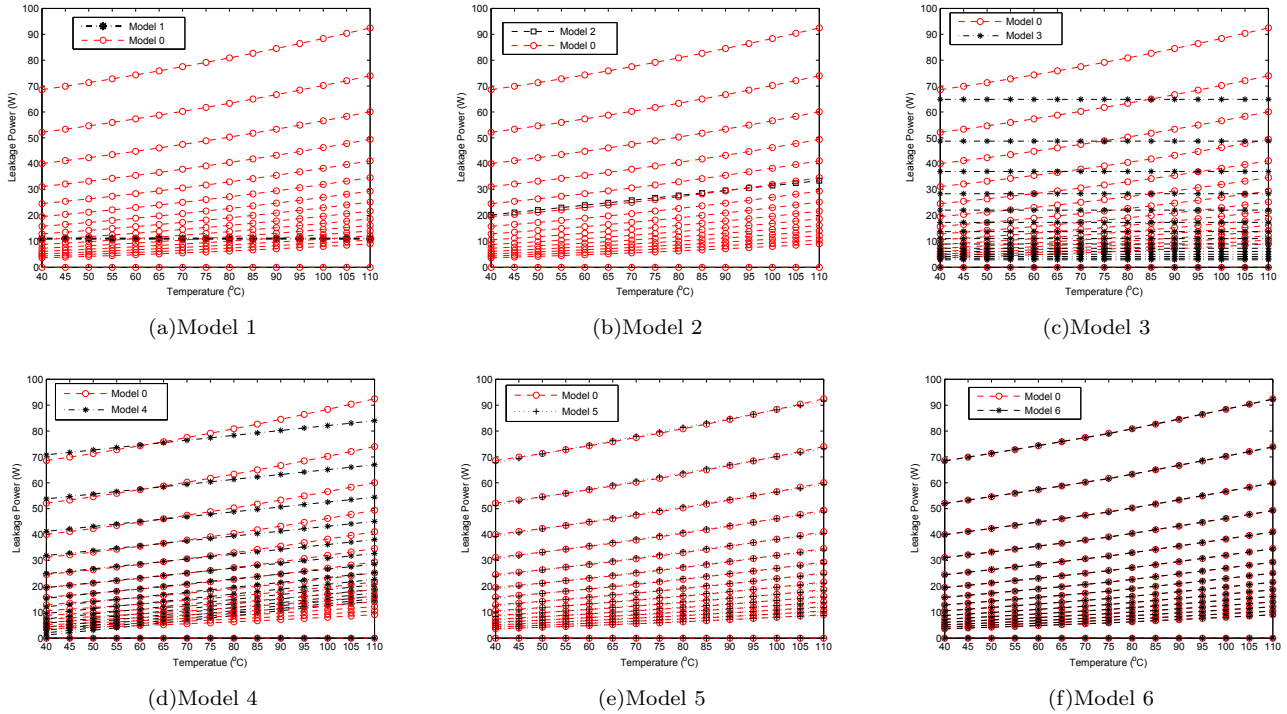
$$AEE(Max) = \max_{i=1}^{k} AEE(M_i) \quad (20)$$

TABLE II
THE ABSOLUTE (AEE) AND RELATIVE (REE) ESTIMATION ERRORS OF LEAKAGE POWER ($Watt$) CONSUMPTION BY DIFFERENT LEAKAGE MODELS.

Model #	M1	M2	M3	M4	M5	M6
AEE(Avg)	28.6	16.1	7.5	1.4	0.24	0.06
AEE(Max)	81	60	27.6	7	0.84	0.2
REE(Avg)	55%	99%	33%	9.5%	1.3%	0.3%
REE(Max)	200%	450%	67%	65%	7.0%	1.5%

From Figure 1 and Table II, we can conclude that leakage models without considering the leakage/temperature dependency or the leakage/supply voltage dependency can lead to very large estimation errors. As illustrated in Figure 1(a) and 1(b), Model 1 and 2 intend to estimate leakage power consumption using one single line instead of a group of lines as other models and thus cause large estimation errors. Even though Model 3 takes the leakage/supply voltage dependency into account, it ignores the leakage/temperature dependency. The estimation errors are still very substantial. Therefore, these three models can be applied only when the supply voltages and temperatures are allowed to varied in a much smaller range. For example, when we limited the processor supply voltage to be within $[1.05, 1.1]V$, we found that the maximum REE by model 3 can be cut to within 8%.

When incorporated with both temperature and supply voltage dependency, the accuracy of a leakage model (e.g. Model 4, 5, and 6) can be dramatically improved as shown in Figure 1(d), 1(e), 1(f) and Table II. Even though at some extreme case, the maximum relative estimation error by Model 4 (i.e. 65%) is similar to that by Model 3 (i.e. 67%), Model 4 is a much more accurate model than Model 3 for average cases as shown in Table II and also Figure 1(d). When we further limited the supply voltages to be within [0.85-1.05]V, the maximum relative error was reduced to 16% and average error became 4.3%. Model 5 is the most accurate single linear approximation model according to our experimental results. We found that the maximal relative estimation error appeared at the lowest supply voltage and temperature. This is because the absolute value of the leakage power at these points are small. Thus a small difference can cause a much larger relative error. To further improve the accuracy, using the piecewise linear (PWL) leakage model (i.e. Model 6) is a viable way. As shown in Fig.1(f), the 2-segment PWL model almost perfectly matches the non-linear leakage power. The average relative error is 0.3% and the maximum relative error is only 1.5%.



(a)Model 1 (b)Model 2 (c)Model 3

(d)Model 4 (e)Model 5 (f)Model 6

Fig. 1. Estimated Leakage power consumption by different leakage models under different temperature and supply voltage.

TABLE III
THE ABSOLUTE (AEE) AND RELATIVE (REE) ESTIMATION ERRORS OF PEAK TEMPERATURE (^oC) BY DIFFERENT LEAKAGE MODELS.

Model #	M 1	M 2	M 3	M 4	M 5	M 6
AEE(Avg)	15	14	9	3.6	1.19	0.57
AEE(Max)	59	47	16	6	1.8	0.9
REE(Avg)	18%	27%	6.6%	3.4%	2.9%	1.5%
REE(Max)	50%	40%	16%	11%	4.8%	2.4%

C. Peak temperature estimations

To study how different leakage models may affect the thermal aware system level analysis, we conducted the second set of experiments. We simulated the scenario when the processor runs at a constant speed long enough until its temperature becomes stable (i.e. temperature variance within 0.001^0C). We collected the peak temperatures estimated based on each model for different supply voltages. The results are depicted in Figure 2. Similarly, we collected the absolute estimation error (AEE) and relative estimation error (REE) for each model and filled in Table III.

As we can see in Figure 2, the peak temperature calculated based on different leakage models demonstrates dramatic differences. When modeling the leakage as a constant, Model 1 can lead to a temperature discrepancy of 15^oC in average, and as much as 59^oC. Even though Model 2 and Model 3 take into account the leakage/temperature and leakage/supply voltage, respectively, the peak temperature discrepancies are still 14^oC and 9^oC in average, and can be as higher as 47^oC and 16^oC, respectively. It is reported that 10^oC increase in temperature can result in 50% reduction in the component's life span [7]. Therefore, the large error margins by Model 1, Model 2, and Model 3, seem to make them inappropriate in system level thermal analysis. On the other hand, the estimated peak temperatures based on Model 4, 5, and 6 match that by Model 0 much closer, as shown in Figure 2. The absolute error by Model 4 is 3.6^oC in average, and 6^oC at most. The results by Model 5 and Model 6 are very close to Model 0, with less than 1.8^oC of absolute error. Our experimental results strengthen the critical role that the leakage power plays in the system level analysis. These results also highlight the fact that, in deep sub micron domain, it is not only important but necessary to take the leakage/temperature and leakage/supply voltage dependency into considerations for high level power and thermal aware system level design.

V. Conclusions

The exponentially increased power consumption has imposed tremendous challenges on both power conservation and heat management problems. When dealing with both problems, the leakage power plays a critical role as the transistor size continues to decrease. High power consumption causes high temperature, which increases leakage power and subsequently the overall power consumption. This positive feedback loop between the leakage and temperature must be addressed properly in high quality electronic system design.

In this paper, we study a large spectrum of leakage power models that can account for the leakage/temperature de-

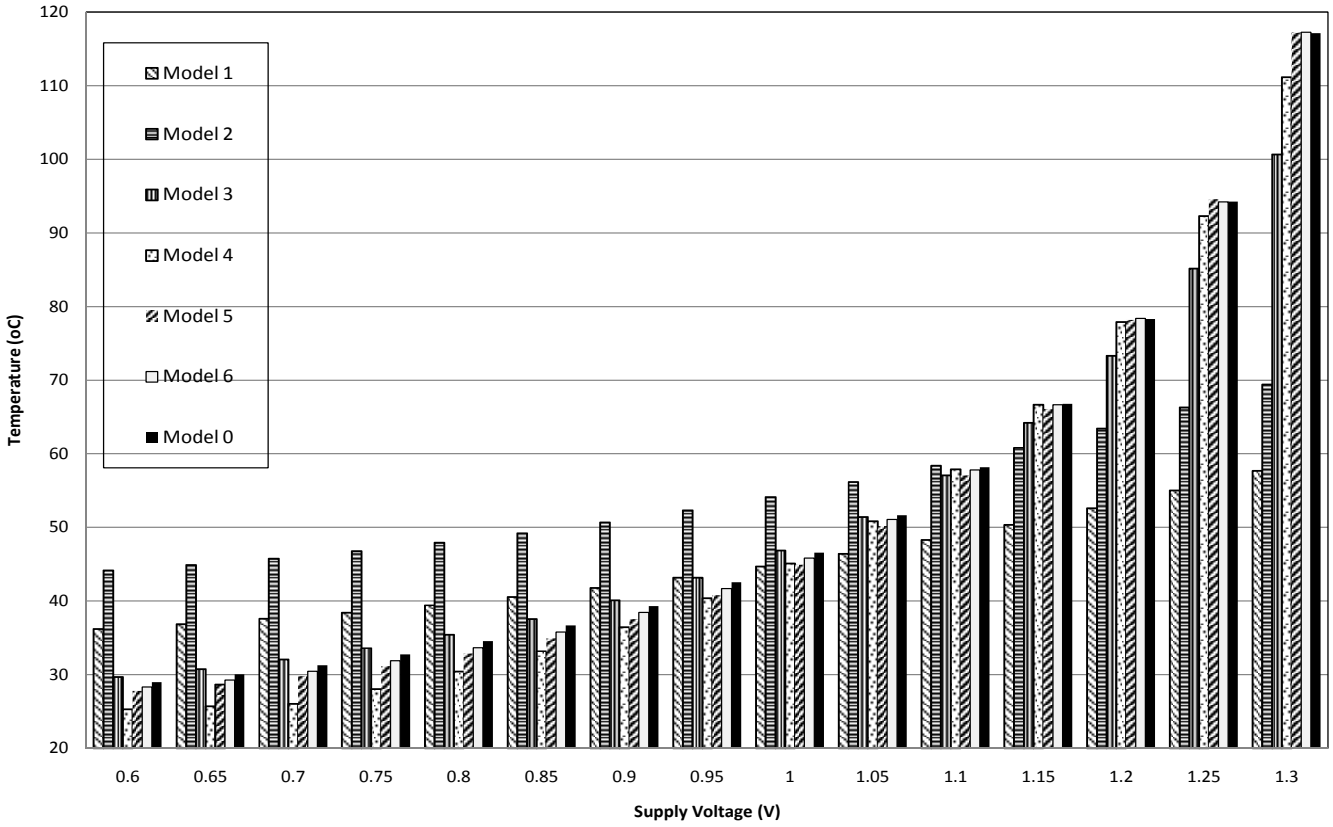


Fig. 2. **Estimated peak temperature for different leakage models**

pendency, and in the meantime, greatly simplify the complex non-linear relationship implied by previous circuit-level researches. We analyze and compare the tradeoffs between the complexity and accuracy for these models empirically. Our experimental results strengthen the critical role that the leakage plays in the system level analysis. More importantly, our results highlight the fact that it is vital to take the leakage/temperature and leakage/supply voltage dependency into considerations for high level power and thermal aware system level design.

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