Communications via Systems-on-Chips Clustering in Large-Scaled Sensor Networks

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Abstract—In this paper, we have proposed a framework of systems-on-chips clustering in application to complicated sensor networks. The framework can be applied to address the communication issues in distributed and large-scaled sensor nodes in wireless sensor network application. There are two communication categories under consideration, i.e. intra-nodes and inter-nodes. Due to the potentially higher frequency in the signal propagation within the sensor node, the characteristics of the interconnect among various systems-on-chips cannot be described in the traditionally lumped R, L, C components. We adapt a distributed transmission line model to address such issues and possibly improve the reliability in the intra-nodes communication. Furthermore, based on the bandwidth requirements of each sensor node, the large-scaled sensor network is proposed to be transformed into a maze diagram by a user defined threshold bandwidth, so that many existing approaches may be applied to determine the routing paths in the inter-nodes communication to improve the efficiency of the overall network.

Index Terms—Sensor networks, Systems-on-chips, Clustering, Maze routing.

I. INTRODUCTION

A sensor is a low-cost and low-power device capable of communicating between short distances. Sensors have been used to collect a wide range of data, including temperature, humidity, pressure, noise levels, vehicular movement, etc. With advancements in digital electronics and wireless communication technologies, sensors have become increasingly powerful and cost effective. It is understood that a possible implementation method for sensor networks could utilize Systems-on-Chips (SoC) designs as sensor nodes.

In the evolution of silicon chips, the technology roadmap [1] states that at 65 nm and below, the design of a very complex chip will consist of billions of transistors operating below 1.0 V with an operational frequency of 10 GHz, which will become a reality by the end of the decade. This rapid migration to nanometer design processes has benefited chip design significantly, where multiple components or subsystems are integrated, sustaining Moore’s Law [2] through scaling technology into the nanometer regime. This will allow for more complex systems utilizing several hundreds of embedded components all on a single chip. Added complexity poses several challenges, including noise, parametric variations, and other device perturbations [3] [4] [5].

Fig. 1 Conceptual Design of SoC Clustering in Sensor Networks

The conceptual design of complicated and multi-purposed sensor system based on SoC clustering is shown in Fig. 1. In the figure, there are several, say six (6), SoC that are clustered together by individual SoC to SoC interconnections (intra-nodes) as a single sensor node in the system. Each SoC is dedicated potentially to one sensor device for desired detection, such as a surveillance device. The responsibilities of the SoC clustering include data transmission, resource allocation, and security, etc., which are all managed on a hardware and middleware level within the sensor node. All sensors have the ability to transfer real-time collected data through the node to the sink (central node) for processing and storage.

As one may notice, the clustering framework, in fact, is similar to the functionalities of a highly scaled VLSI silicon chip with multi-cored environments. In other words, each SoC has its own processor as a computational core plus other resources, such as memory, interrupts, timers, and I/O modules. Since they are all collectively within a single chip (i.e. single sensor node in SoC clustering platform), the resources may be shared, reconfigured, and distributed among other processors or cores.

One important issue in such a design is the communication among these SoC systems within the sensor node, the so-called intra-nodes communication. The frequency of such intra-nodes communication is expected to exceed 15 GHz in 2010 [6].
and 50 GHz in 2020. The challenge in this area is to use an accurate, low-power and high-speed signal transmission model.

It is understood that when the switching speeds of the chips become sufficiently fast, the inductance of the wire among SoC starts to dominate the delay behavior [8]. This means that the rise and fall times of the signal itself becomes comparable to the time of the propagation of the signal across the interconnect wires. Hence, the modeling of transmission is needed to describe such a behavior.

II. MODELING OF INTRA-NODE COMMUNICATION

A. Review of Lossless Digital Transmission Line

Digital signal consists various frequency components that cover wide frequency spectrum. At higher frequency, all R (or G), L, C parameters become frequency-dependent. The transmission line modeling consists of the prime property that a signal propagates over the interconnected media with the functionalities like wave [8]. Therefore, an accurate model, which can handle signals with the distributed properties of R, L, and C, are needed for digital transmission line design in SoC clustering systems in sensor networks.

Consider the point x along the transmission line at time t. The following equations should hold:

\[ \frac{\partial v}{\partial x} = -ri - l \frac{\partial i}{\partial t} \]  
\[ \frac{\partial i}{\partial x} = -gv - C \frac{\partial v}{\partial t} \]  

where \( v \) and \( i \) denote voltage and current, respectively. Assume that the leakage conductance \( g \) equals to 0, and eliminate the current \( i \), the wave propagation equation can be written as

\[ \frac{\partial^2 v}{\partial x^2} = rc \frac{\partial v}{\partial t} + lC \frac{\partial^2 v}{\partial t^2} \]  

where \( r, c, \) and \( l \) are the resistance, capacitance, and inductance per unit length, respectively.

For a lossless transmission line, the characteristic impedance \( Z \) of the line is a function of the dielectric medium and the geometry of the conducting wire and isolator that is independent of the wire length and frequency [8][7]. Hence, it can be written as

\[ Z = \sqrt{\frac{\mu}{\varepsilon}} \]  

where \( \varepsilon, \mu, \) and \( c \) are the permittivity, permeability of the surrounding dielectric and the capacitance per unit length of the wire, respectively.

B. Lossy Digital Transmission Line

In reality, the digital transmission line cannot be considered as lossless. The design rules of thumb [8][9] are:

1. \( rc \) delays should be considered only when the propagation delay of \( rc \) is comparable or larger than the propagation delay of the driving gate.

2. \( rc \) delays should only be considered when the rise or fall time at the line input is smaller than the total rise or fall time of the wire.

Hence, in consideration of the intra-nodes communication, such lossy transmission line modeling is essential because of the increasing frequency approaching to 10-50 GHz or above in the near future [1][6].

III. MODELING OF INTER-NODES COMMUNICATION

A. Routing Algorithm

The conceptual modeling of inter-nodes communication is to address the issues in connecting distributed and large-scaled sensor networks, other than the communications within a sensor node (intra-nodes communication). A large scaled network of sensor nodes capable of communicating with each other provides significant new capabilities for automatically collecting and analyzing data from physical environments. This notable deployment of these networks is that these nodes are strictly distributed randomly to cover a given region, which permits the network to provide reliable transmission, prolong the effective signaling time, and tolerate unavoidable errors.

In this paper, we adapt an algorithm to avoid the nodes with high-bandwidth requirements based on the well known Maze routing [10] due to its ability of solving congestion flow and bottleneck problem. It is because that this algorithm may provide an optimum routing path without causing the reconfiguration of the network. However, one shall notice that the solution to such maze problem is not unique. We simply use a well-known algorithm as an example.

The concept of such an algorithm works like this. The Maze routing is assumed to occur in a unit-size grid. The algorithm works in two phases [11]. First, points on the grid are iteratively labeled with their distance from a source point. Second, a route is traced back from the sink to the source. It means that the route is drawn, so that it never goes to a point with a higher-order label.

In our routing modeling of inter-nodes communication, we label every node based on the required bandwidths. We set a cutoff bandwidth as a threshold value to determine the high or low label in each node. The idea is that we want to avoid the nodes that are "bandwidth-hungry" to avoid potential congestion in the network. The threshold can be adjusted by the designer to make the overall network more efficient. Hence, the determination of bandwidth requirement is crucially important in designing such a large-scaled network.
B. Bandwidth Estimation in Sensor Nodes

As shown in Fig. 2, the encoder architecture in SoC, such as H.264, can be decomposed into several components. Given a sensor node, the bandwidth estimation can be obtained depending upon the number of SoC components [12]. Based on SoC architecture, such as H.264, we can assume the system bus bandwidth \( B_{sys} \) cost function as [12]:

\[
B_{sys} = C + I + O + H
\]

where \( C, I, O, \) and \( H \) denote the bandwidths between CPU processors (cores), sensory input data, sensory/control output data, and H.264 Codec core and memory, respectively.

\( C \) exists in every system since it is the control line from the CPU cores. Every application may have different \( C \) in modeling. The \( I, O, \) and \( H \) are all connected to the memory side. Hence, the bandwidth of the memory should be \( B_{mem} = I + O + H \).

Specifically, the \( I \) is the input source of the system. In Real Time specific H.264 application, it stands for the input source of the video data from the sensor or camera. The \( O \) component is the output compressed data of the encoder. In general, \( O \) is the result of \( I \) compressed with H.264 algorithm and \( O \) is much smaller than \( I \), usually about 1/50 or 1/100. As the bandwidth goes really high in the H.264 CODEC, maybe several times, or even several tens of times of \( I, O \) can be neglected. Hence, \( H \) is the dominant term which affects the bandwidth of SoC.

![H.264 Encoder Architecture](image)

Through such an approach, we may estimate the bandwidth of each SoC [12]. Once we estimate the overall bandwidth in each sensor node, a cutoff bandwidth as the threshold can be intuitively determined by the designer for the most efficiency of the overall network. Based on such a threshold, the routing maze can be created. Applying appropriate routing algorithms will result in the most efficient path of transmitting data from the source to any given destination.

IV. EXPERIMENTAL RESULTS

In this experiment, we implemented our algorithm in the Java programming language on NetBeans IDE 6.1 (Build 200805300101) running on the system of Windows Vista ver. 6.0.

First, we assume that all the sensor nodes with certain bandwidth and frequency are uniformly distributed in a very large networks. In each sensor node, given the threshold bandwidth as a cutoff bandwidth (or called cutoff frequency), we select the node with lower frequency and bandwidth to reduce the power consumption and balance the congestion control. The idea is that we will try to travel the routing path along with the nodes with lower bandwidth to avoid the traffic congestion, and avoid to pass onto the nodes with higher bandwidth requirements.

Second, we generate the maze diagram composed by the number of cells representing sensor nodes in the network. As examples in Fig. 3 and Fig. 4, the left upper corner is the starting node \( A \), which tries to traverse the maze to the ending node on the lower right corner node denoted as \( B \). If the neighboring node broadcasting with high frequency, we will use 0 to draw a wall from \( A \) to its neighboring nodes, otherwise we will use 1 to keep it blank in the maze diagram to represent the nodes with high frequency and bandwidth. Our goal is to traverse the maze from \( A \) to \( B \) by choosing the path of passing nodes with lower frequency, such that the traffic congestion can be avoided.

In our experiment, we use depth-first search and the right (or left) wall rule to find the path and then mark the visited nodes. We will keep on moving until reaching a wall or a dead-end, and then trace back to the nearest cell, where there is another path available to pick.

The overall algorithm is shown as follows:

1) Traverse Maze From A to B: mark a wall when nodes with high frequency
2) if the current cell is B, then return true to terminate the loop to indicate a solution has been found if the current square is marked, return false to indicate this cell has been tried
3) add the current cell to the stack
4) for (left, right, up, down)
if (any of direction not blocked by a wall) 
moves to that direction from the current cell 
repeat the step by recursively calling the function 
5) if current cell reached B, the return "true" to terminate 
the loop to solve the maze 
6) remove the last current cell from stack 
7) return "false" to indicate that choosing this cell will not 
lead to the destination cell 

By applying this algorithm, we may find at least one routing 
path that is the most efficient in terms of bandwidth cost for 
inter-nodes communication in the overall network, as shown 
in Fig. 3 and Fig. 4.

At a given cutoff frequency, Fig. 5 and Fig. 6 show the 
maze diagrams with 2,500 sensor nodes and 10,000 nodes, 
respectively. By adapting an appropriate routing algorithm, 
we may draw a routing path that avoids crossing the nodes with 
high bandwidth requirements.

V. CONCLUSION

The proposed framework in systems-on-chips can be applied 
to address the communication issues in complicated and large-
scaled sensor nodes in wireless sensor network application. 
In intra-nodes communication, the modeling of distributed 
transmission line should be used to address the issues of 
higher frequency in the range of up to several GHz. In inter-
nodes communication, a maze diagram is created with a given 
threshold bandwidth to avoid the potential congestion spots 
with appropriate routing paths, such that the overall network 
efficiency can be improved. Experiments show an example of 
the large size of sensor networks up to 10,000 sensor nodes 
by using such a maze diagram.

REFERENCES

[1] "International technology roadmap for semiconduc-
tors," (2003), ITRS 2003 Edition, [Online], available: 
http://www.intel.com/technology/silicon/mooreslaw/
[4] N. Sano, "Increasing importance of electronic thermal noise in sub-
0.1mm Si-MOSFETs," IEICE Transactions on Electronics, vol. 83, pp. 
1203-1211, 2000
micro and nano electronics," Physics Letter A, vol. 305, pp. 144-149, 
2002.
[6] "National technology roadmap for semiconductors," Semiconductor In-
trical signaling,” in IEEE Int. Conf. on Massively Parallel Processing 
364-365, 1961
Embedded Software and Systems (ICESS’08), pp. 277-282, Chengdu, 
China, July 29-31, 2008