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Parameterized Interconnect Modeling and Simulation in VLSI Design Considering Variations

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Abstract

This paper proposed a new algorithm for modeling and simulation of interconnect circuit in nanometer Very Large Scale Integration (VLSI) design considering manufacturing process variations. The approach is based on the existing Passive Reduced-order Interconnect Macromodeling Algorithm (PRIMA). By satisfying the constraints of PRIMA, both macromodel stability and passivity are preserved, so that overall circuit stability is guaranteed for active driver and passive load interconnect circuits. As a result, transfer function of interconnect circuit under the influence of process variation is obtained, where reduction matrix is calculated once only for different values of parameters describing characteristics of process variations. Experiments demonstrate that result from proposed parameterized PRIMA considering process variation is very close to that obtained from PRIMA, while execution time is much less (up to 512X faster).

1. Introduction

Being able to find the characteristics of interconnect circuit is critical in chip design. As the speed of chip increases, delay of interconnect circuit becomes more important. Also, several assumptions about interconnect circuit design become invalid as chips are manufactured at the scale of nanometer and the operation frequency is raised to the GHz range. Impedance of Inductance, which is a function of frequency, is not negligible anymore and its contribution to delay and signal integrity is a major concern in chip design. Furthermore, effects of process variation cannot be ignored as the size of chip is getting smaller. When process variation is considered [3], difference of about twenty percent is introduced in timing analysis, leakage power analysis, chip white space and power consumption. Therefore, successful chip design depends on more than just delay, where a better understanding of the shape of signals is required. As a result, this paper suggests an approach to efficiently solve for the transfer function of passive interconnect circuit under the influence of process variation.

Node voltage and branch current of interconnect circuit can be solved using Modified Nodal Analysis (MNA) equations. Although MNA techniques give an exact solution to the problem, the complexity of solving MNA equations grows exponentially with the number of elements in the circuit. For each new node added to the circuit, the capacitance and conductance matrices grow in both dimensions. In order to quickly solve MNA equations, the system is reduced to smaller dimensions so that accuracy is traded off for quicker execution time. PRIMA is one of the model order reduction techniques and it generates provably passive reduced order N-port models for RLC interconnect circuits. As a result, one is guaranteed to get stable solutions and faster simulation time by using PRIMA to solve MNA equations.

Although most model order reduction techniques solve MNA equations efficiently, the reduction matrix used to reduce the system has to be re-calculated every time any value of the capacitance and conductance matrices is changed. This will induce a large overall execution time for optimizing the size of an interconnect circuit, where the values of capacitance and conductance greatly depends on the physical dimension of wires. Some researcher [1] suggests a parameterization technique in which variables such as length, width and height of wire are modeled as parameters of MNA equations, so that the reduction matrix is calculated once and it can be used for any value of the parameters. However, solution of the technique is not guaranteed to be stable and the order of approximation is limited.

2. Design of parameterized MOR considering variation

This section is going to briefly describe the model order reduction technique of PRIMA [2] as well as the parameterization technique suggested in [1]. At the end, ideas of the proposed parameterized PRIMA considering process variation are introduced.

2.1 PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm

In reality, reduced model of a system is connected with others and circuit elements so that the whole system can be simulated efficiently. It is importance that the system to be reduced is passive; otherwise, energy could be generated within the system itself and the output will be unbounded. More important, interconnect of passive systems will be a passive one, while interconnect of stable model does not guarantee that the resulting model to be stabilized. As a result, PRIMA introduces a technique so that the passivity of the original system is retained and stable solution can be generated. Given that a system is described by MNA:

$$C\dot{x}_n = -Gx_n + Bu_p$$

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$$i_p = L^T X_n \quad (1)$$

where i_p and u_p denote the port current and voltage respectively and

$$G \equiv \begin{bmatrix} N & E \\ -E^T & 0 \end{bmatrix} \quad C \equiv \begin{bmatrix} Q & 0 \\ 0 & H \end{bmatrix} \quad x_n \equiv \begin{bmatrix} v \\ i \end{bmatrix} \quad (2)$$

Where **v** and **i** are the MNA variables corresponding to the node voltages, inductor and voltage source currents respectively. The *n x n* matrices **G** and **C** represent the conductance and susceptance matrices. **N**, **Q** and **H** are the matrices containing the stamps for resistors, capacitors and inductors respectively. **E** consists of ones, minus ones and zeros, which represent the current variables in KCL equations.

PRIMA preserves the passivity of the system by using Arnoldi algorithm so that the pair of reduction matrices is equivalent and the projection becomes a congruence transformation. Also, the input matrix **B** is equal to the output matrix **L**. Finally, PRIMA applies the reduction matrix **X** directly to **G** and **C** to match the first q/N moments so that in brief:

$$\begin{gathered} \mathrm{colsp}(X) = \mathrm{Kr}\left(A, R, \left\lfloor\frac{q}{N}\right\rfloor\right) \\ X^T X = I_q \\ X_n = X_{\{nxq\}} X_q \\ (X^T C X)\tilde{x}_q = -(X^T G X)\tilde{X}_q + (X^T B)u_p \\ i_p = (L^T X)\tilde{X}_q \end{gathered} \quad (3)$$

where the reduced order MNA matrix are:

$$\tilde{C} = X^T C X \quad \tilde{G} = X^T G X \quad \tilde{B} = X^T B \quad \tilde{L} = X^T L \quad (4)$$

Therefore, a passive system described by MNA equations can be solved efficiently and the solution is guaranteed to be stable.

2.2 A multiparamter moment matching model reduction approach for generating geometrically parameterized interconnect performance models

Design of interconnect circuit in order to minimize certain circuit characteristics such as delay, skew and power consumption often requires varying the size of wire several times so as to find the optimized solution. Observing that the cost of computation is high for extracting even a modestly accurate model of a wire, this paper applies a parameterized reduced order interconnect model to provide a feasible solution to their size optimizing interconnect problem. Given that a system is described by E with u parameters where **u** and **y** are the input and output of the system respectively: $E(s_1, \dots, s_u)x = Bu$

$$y = Cx, \quad (5)$$

B and **C** are the input and output matrices respectively. A power series expansion for all parameters can be obtained for the system in a general form as follows:

$$E(s_1, \dots, s_u) = E_0 + \sum_i s_i E_i + \sum_{h,k} s_h s_k E_{h,k} + \sum_{h,k,j} s_h s_k s_j E_{h,k,j} \; () \quad (6)$$

Therefore, the system can be re-written as:

$$\left[E_0 + \tilde{s}_1 E_1 + \cdots + \tilde{s}_p E_p\right]x = Bu$$
$$y = Cx \quad (7)$$

Finally, the resulting system can be solved efficiently using parameterized reduction matrix V:

$$[V^T E_0 V + \tilde{s}_1 V^T E_1 V + \tilde{s}_p V^T E_p V]\tilde{x} = V^T Bu$$
$$y = CV\tilde{x} \quad (8)$$

As a result, the approximation of the system is based on the matrices related to parameters. V is generated once only so that solving subsequent MNA equations with changes of parameters can be solved efficiently.

2.3 Proposed parameterized PRIMA considering process variation

The proposed algorithm makes use of the parameterized model order reduction technique with the PRIMA technique so that the solution will be stabilized and MNA equations with changes of process variation parameters can be solved efficiently. First, process variation is modeled as parameters and they are introduced in the traditional MNA equations. Second, the system is subjected to power series expansion so that the reduction matrix is calculated. Finally, all these changes are adapted in PRIMA. Implementation details are described in Section 3.

3. Implementation of the proposed algorithm

Parameterized PRIMA considering process variation tries to parameterized process variation effects in MNA equations and then they are solved by PRIMA to generate stable solution efficiently. First, each source of process variation, either for resistance, capacitance or inductance, is represented by a random variable and a corresponding matrix which described the circuit element it affects. Since process variations effects are generally increasing or decreasing the values of circuit elements, they are modeled as linear effects on the MNA equations as shown below:

$$\left(G + \sum_{k=1}^{m} rg_k G_k' + s\left[C + \sum_{j=1}^{n} rc_j C_j'\right]\right)X = B$$
$$Y = L^T X \quad (9)$$

where the conductance matrix G, susceptance matrix C, state variable vector X, input mapping matrix B, output mapping matrix L and output matrix Y preserve their original meanings. There are m number of sources of process variation for conductance, where each is represented by a random variable rg_k and the corresponding matrix G_k'. The product of the two should give the variation of certain circuit elements affected by a particular source of process variation. Similarly, there are n number of sources of process variation for inductance and capacitance, where each is represented by a random variable rc_j and the corresponding matrix C_j'. Particularly, G_k' and C_j' are chosen to be the maximum values of circuit elements for a particular process variation source and rg_k and rc_j are within the range of plus and minus one.

The frequency variable s and all rg_k and rc_j are treated as parameters, starting from s_1 to s_u respectively. Since there are m plus n sources of process variation, the total number of u is m + n + 1. Therefore, Taylor expansion of the MNA equation is calculated. As rg_k and rc_j are expanded around zeros, which is a reasonable assumption since the solution considering process variation is approximated as a derivation from that without considering process variation; the expansion can be simplified as follows:

$$E(s_1, \ldots, s_u) = G + \Delta s_1 G + \Delta s_2 G_1' + \Delta s_2 G_1' + \Delta s_3 G_2' + \cdots + \Delta s_{m+1} G_m'$$
$$+0s + 0s + \Delta s_{m+2} \Delta s_1 C_1' + \Delta s_{m+3} \Delta s_1 C_2' + \cdots + \Delta s_{m+n+1} \Delta s_1 C_n' \quad (10)$$

Where Δs are the difference between the actual values of parameters being used and the expansion points, hence, they are further simplified as just the actual values of parameters. Also, following the notation from the parameterization technique suggested in [1], matrices including G, C, G_k' and C_j' in each of the terms of the Taylor expansion corresponds to one E term. As a result, B_m and M terms are calculated as follows:

$$B_m = \widetilde{E}_0^{-1} B$$
$$M_1 = -\widetilde{E}_0^{-1} \widetilde{E}_1$$
$$\vdots$$
$$M_{m+n+1} = -\widetilde{E}_0^{-1} \widetilde{E}_{m+n+1} \quad (11)$$

And the column span of the reduction matrix for first order approximation is:

$$\mathrm{colspan}(V) = \mathrm{span}(b_M, M_1 b_M, M_2 b_M, \ldots, M_p b_M) \quad (12)$$

For the second order approximation, the reduction matrix is:

$$\mathrm{colspan}(V) = \mathrm{span}\left\{\begin{matrix} b_M, M_1 b_M, M_2 b_M, \ldots, M_p b_M, \\ M_1^2 b_M, (M_1 M_2 + M_2 M_1) b_M, \ldots \\ \ldots, (M_1 M_p + M_p M_1) b_M, \\ M_2^2 b_M, (M_2 M_3 + M_3 M_2) b_M, \ldots \end{matrix}\right\} \quad (13)$$

As discussed in [1], the size of the reduction matrix grows exponentially as the order of approximation increases. Therefore, this paper suggests the maximum order of approximation to be the second order.

Finally, all these concepts are employed in PRIMA. Figure 1 shows the pseudo code for parameterized PRIMA considering process variation. Circle bullets are lines of the original pseudo code of PRIMA and square bullets are lines of codes of PRIMA substituted by the approach suggested in this paper. In practice, colspan(V) = {R, AR, A2R,…} of PRIMA is replaced by the colspan(V) as discussed earlier and the definition of Gq = V'GV and Cq = V'CV is substituted by Gq = V'GV + rg_1V'G_1V + …+ rg_mV'G_mV and Cq = V'CV + rc_1V'C_1V + … + rc_nV'C_nV so that the original PRIMA code adapts to parameterized PRIMA considering process variation.

- ○ Connect voltage sources to the multiport & obtain the MNA matrices as in (2)
- ○ Set $[b_1|b_2|\ldots|b_p]$=B and $[I_1|I_2|\ldots|I_p]$=L
- □ Find all the E terms by matching to power series expansion
- □ Find BM and M from all the E terms
- □ Find the reduction matrix V from BM and all the M terms
- □ Orthonormalizing V using Gram-Schmidt
- □ Computer $\widetilde{C} = V^T C V + rg1 V^T G1 V + \cdots$

  $\widetilde{G} = V^T G V + rg1 V^T C1 V + \cdots$
- ○ Find eigendecomposition of $\widetilde{G}^{-1}\widetilde{C}$: $\widetilde{G}^{-1}\widetilde{C} = S \wedge S^{-1}$ *

  $\wedge = \mathrm{diag}(\lambda_1, \lambda_2, \ldots, \lambda_q,)$
- ○ To find poles and residues for $\widetilde{Y}_{i,j}(s)$:

  Solve $\widetilde{G}w = V^T b_j$ for w

  Set $u = S^T V^T I_i$ and $v = S^{-1} w$

  $\widetilde{Y}_{i,j}(s) = \sum_{n=1}^{q} \frac{u_n v_n}{1+s\lambda_n}$
- ○ Set $\widetilde{Y}(s) = \begin{bmatrix} \widetilde{Y}_{1,1} & \cdots & \widetilde{Y}_{1,p} \\ \vdots & \ddots & \vdots \\ \widetilde{Y}_{p,1} & \cdots & \widetilde{Y}_{p,p} \end{bmatrix}$

Figure 1 Pseudo code of parameterized PRIMA considering process variation

4. Experimental results

4.1 Experiment baseline and comparison

The experiments are run with circuits sized 512, 1024 and 2048 elements. In all cases, simulation without reduction and PRIMA matching 2nd moment is performed as a baseline for comparison. With each circuit size the parameterized PRIMA matching 1st and 2nd order with four parameters are executed to evaluate for speed and accuracy.

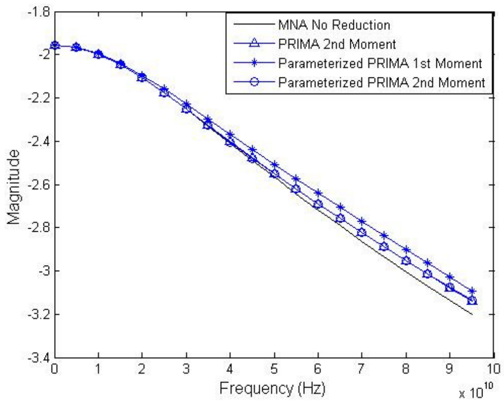

Figure 2: Comparison of Different method of circuit evaluation for circuit size of 2048 G and 2048 C elements.

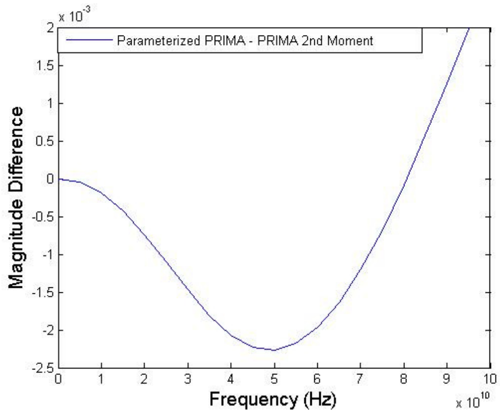

Figure 3: Difference of Parameterized PRIMA and PRIMA 2nd moment.

In Figure 2, we look at the accuracy of our parameterization method without introducing any errors into the MNA matrices. As expected the three methods of PRIMA does not yield an exactly match of the original circuit. Also, the parameterized PRIMA matching 1st moment is not as accurate as the PRIMA and parameterized PRIMA matching the 2nd Moment. What is notable is how closely the parameterized PRIMA matches the normal PRIMA even though they have vastly different reduction matrices. The parameterized PRIMA is about 10 times larger than the regular PRIMA but does not yield considerable improvements. Figure 3 shows the difference between Parameterized PRIMA 2nd moment and PRIMA 2nd moment. Initially the parameterized PRIMA match slightly better, but at higher frequency, PRIMA fared a little better with the gap increasing. However, the order of magnitude of the error makes the difference negligible.

Both the parameterized PRIMA and PRIMA matching 2nd moment again were very close to each other. Closer inspection would show that the two again differ on the order of 10E-3 which is again negligible when considering the magnitude of the reference value. This validates the accuracy of our method. The timing of the different methods will be discussed in Section 0.

Once we were satisfied that our method did indeed match the results of PRIMA we varied the value of one of the four parameters. The G matrix of the original MNA matrices had its corresponding values changed as well. In Figure 4 we show the baseline unchanged MNA output as the solid line and how having 5% change in half of the G matrix changes the output as the dashed line. The parameterized PRIMA matching 1st moment as expected did not match as closely as the others.

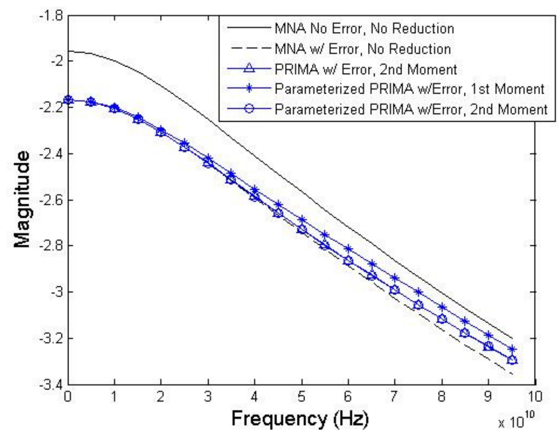

Figure 4: Displays the effects of error and comparison of different method of circuit evaluation for circuit size of 2048 G and 2048 C elements.

4.2 Timing

The time to find the reduction matrix V_t is shown in Figure 5, it is noted that all the reduction method have an exponential complexity in calculating the reduction matrices. PRIMA has the smallest reduction matrix and as expected the parameterized PRIMA 1st moment has a smaller reduction matrix compared to the 2nd moment matching matrix.

When plotting the delay in calculating the reduction matrix (Figure 6) from the smallest to the largest, we observed a polynomial growth pattern in execution time. Following this trend, the delay in attempting to match any higher order moments might approach that of not performing any reduction at all. However, examining the data in Table 1 and the trend shown, the MNA execution time will still out grow the reduction time as the circuit size get larger.

Shown in Figure 7 is the growth of the reduction matrix size verses the number of parameters. A linear line fit of the data in Figure 7 shows a slope of 20 times the number of parameters. For smaller circuits the parameterized PRIMA method will not save much time since matching 2nd moment will bring the reduction matrix size close to the original matrix. Our method is suitable when the ratio of parameters to original matrix size is small.

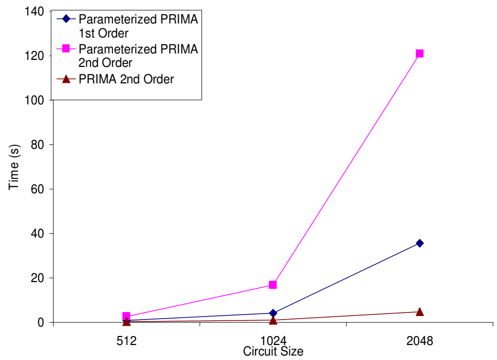

Figure 5: Time to form the reduction matrix.

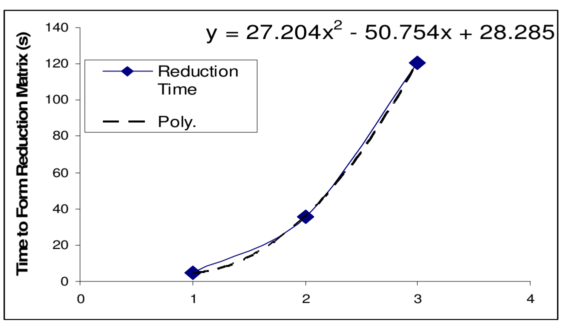

Figure 6: The delay in calculating the reduction matrix as the number of moment to match increases.

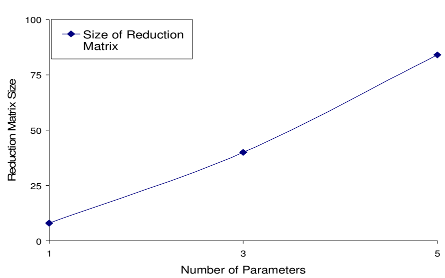

Figure 7: Plot of the reduction matrix size vs. number of parameters.

The total run time shown in Figure 8 again is exponential in nature. For the reduction matrices, the exponential run time is expect since the reduction matrix sizes grows exponentially so the time to evaluate the output will growth exponentially as well. It is obvious that the time saving is enormous by using PRIMA instead of MNA. In tasks such as Monte Carlo simulations, the time saving will make the time spend in finding the reduction matrices worthwhile.

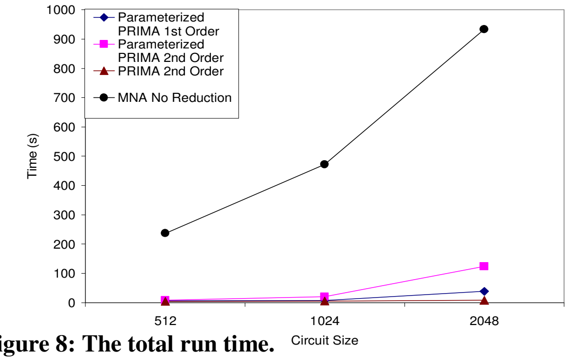

Figure 8: The total run time.

5. Conclusion

In this paper we proposed a method to model process variation using multi-parameter moment matching, specifically multi-parameter PRIMA. Our extension of PRIMA to include additional parameters did not lower the accuracy of the model order reduction compared to reduction via PRIMA. We do see polynomial growth in the time to produce the reduction matrix. The size of the reduction matrix however only grew linearly with respect to the number of parameters. Since process variation at any area of the circuit might be highly correlated to its neighbors. The grouping of similar variations will keep the number of parameters low with respect to the circuit size.

6. References

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